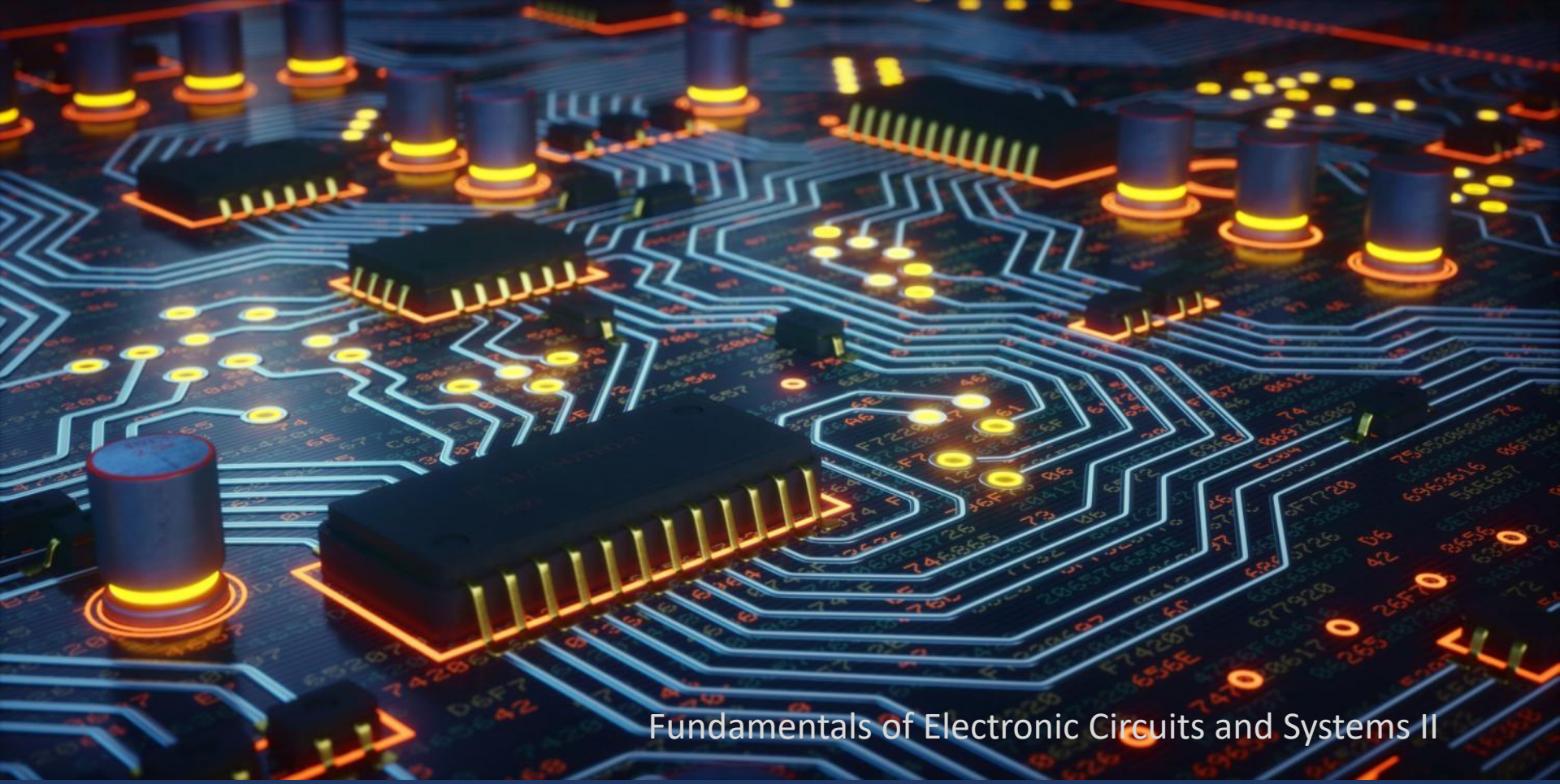

CMOS Digital Logic Circuits

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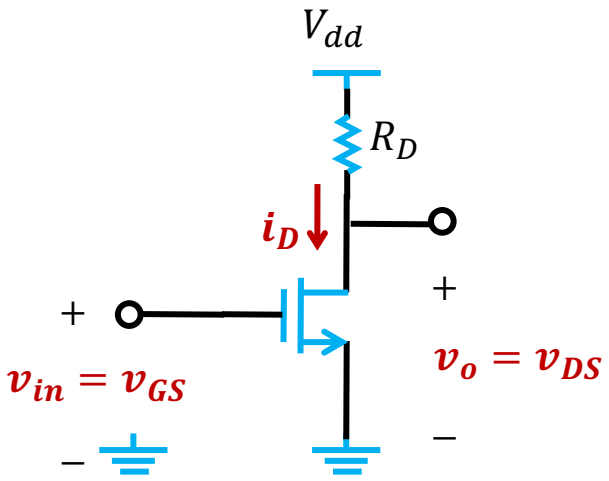
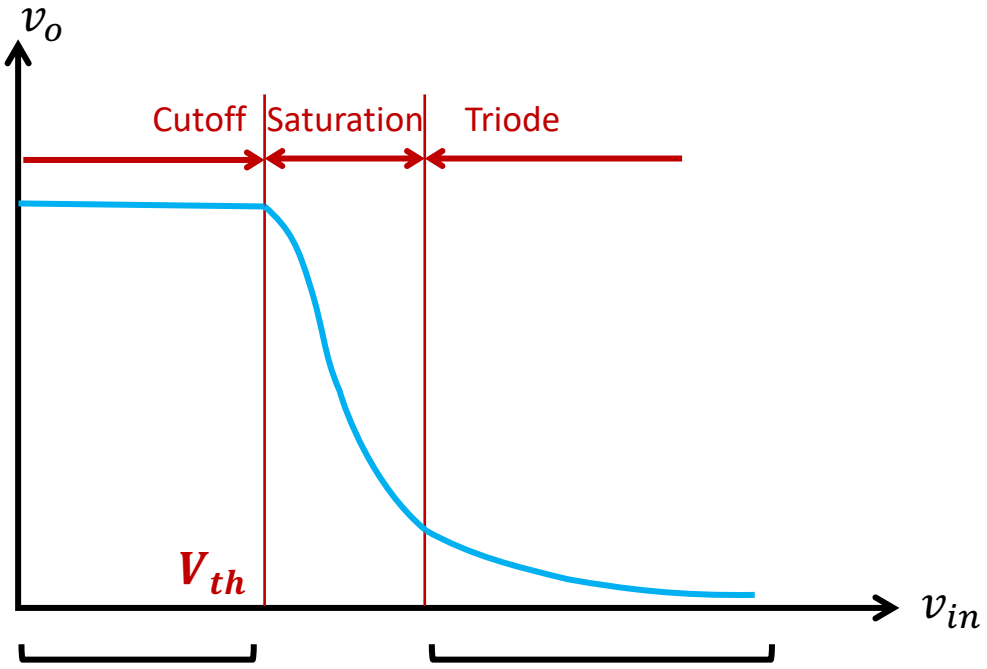
Dept of EE, Tsinghua University

Outline

- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches
- Memory Circuits

Recall: NMOS Transfer Characteristic





$v_{in} < V_{th}$

$i_D = 0$

$v_o = V_{dd} - i_D R_D = V_{dd}$

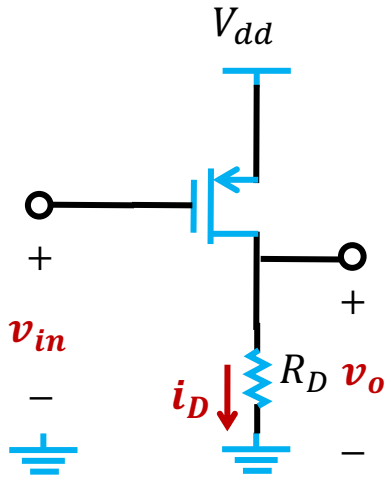
$v_{in} > V_{th}$

$v_{GS} - v_{DS} > V_{th}$

$i_D = k_n \left[(v_{GS} - V_{th}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$

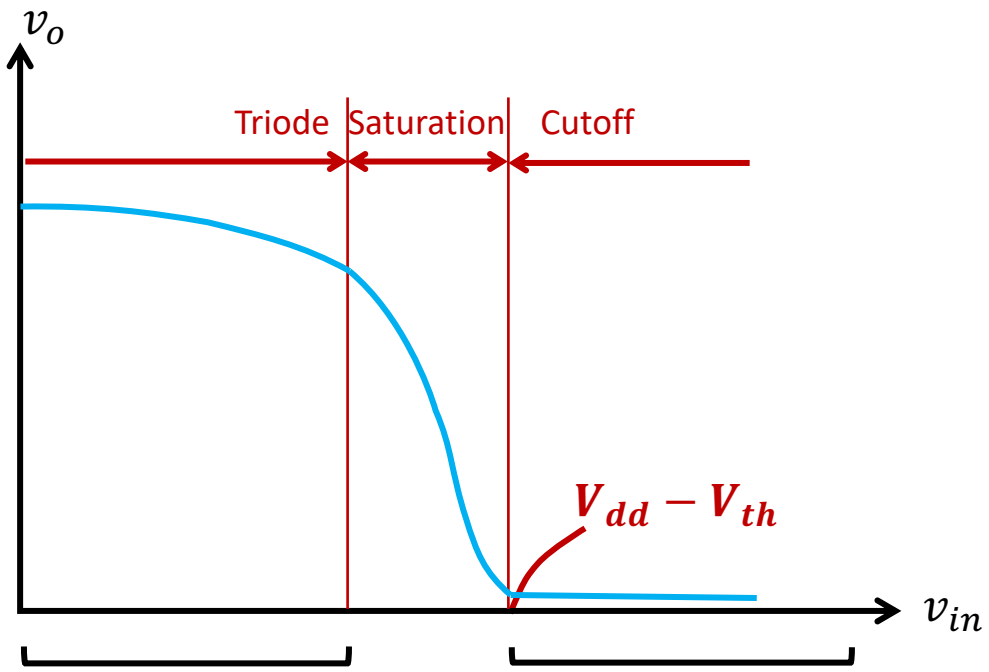
$v_o = V_{dd} - i_D R_D$

How about a PMOS circuit?



$v_{in} = V_{dd} + v_{GS}$

$v_o = V_{dd} + v_{DS}$



$v_{in} < V_{dd} - V_{th}$

$v_{DS} - v_{GS} > V_{th}$

$$i_D = k_n\left[(v_{SG} - V_{th})v_{SD} - \frac{1}{2}v_{SD}^2\right]$$

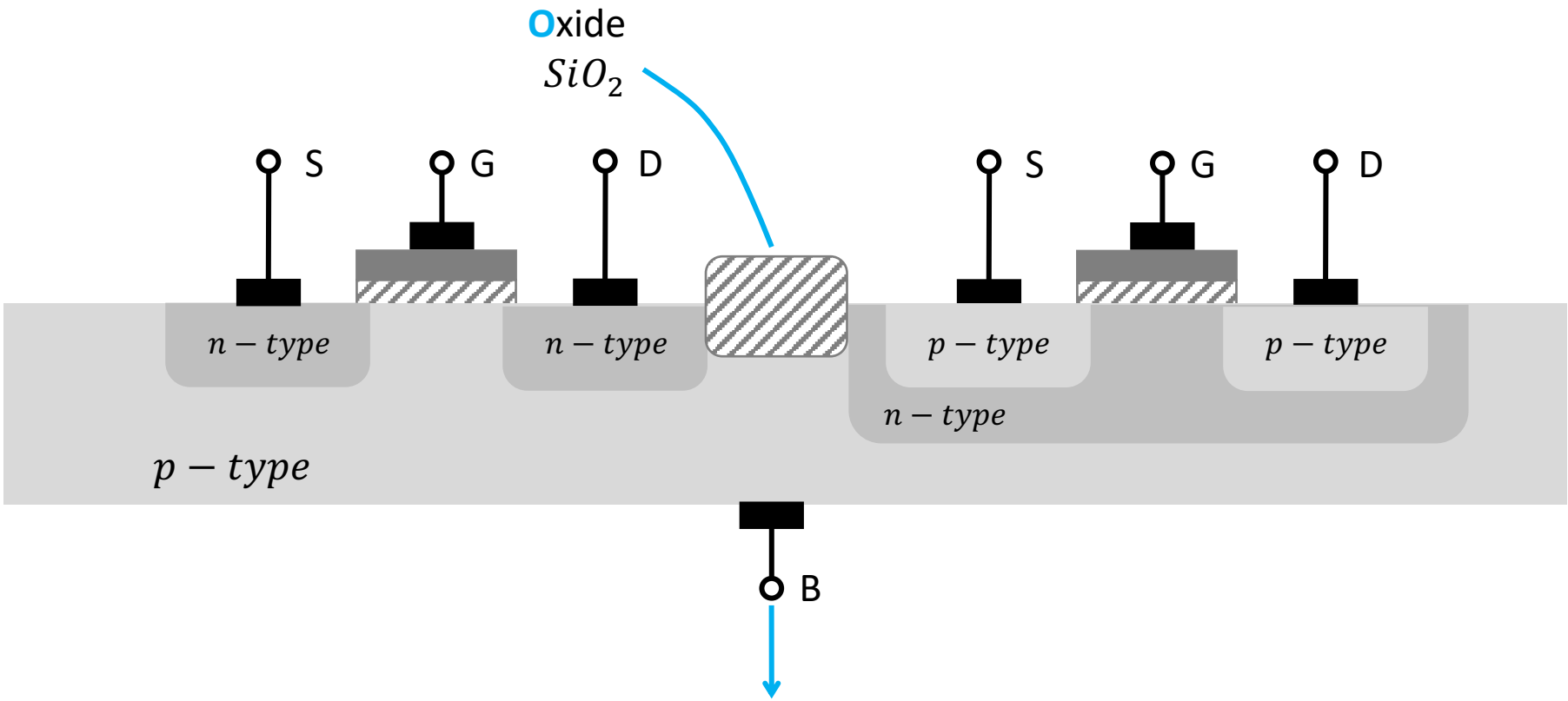
$v_{in} > V_{dd} - V_{th}$

$i_D = 0$

$v_o = i_D R_D = 0$

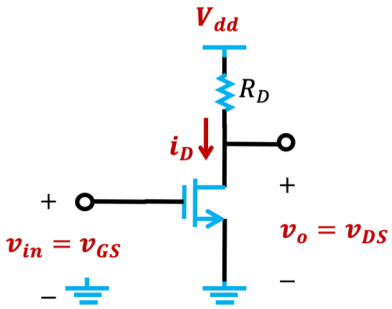
$v_{SD} = V_{dd} - v_o = V_{dd}$

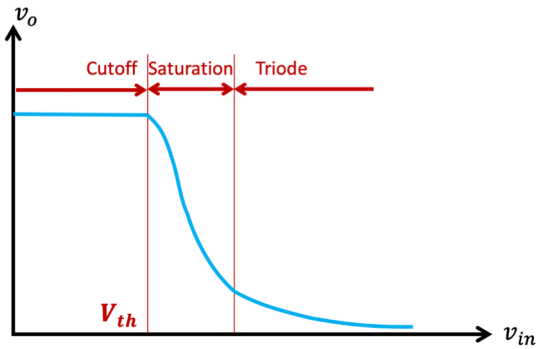
Recall: Complementary MOS (CMOS)

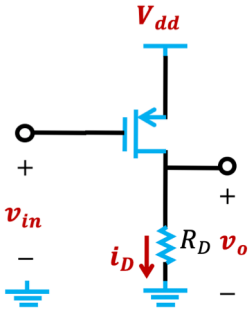


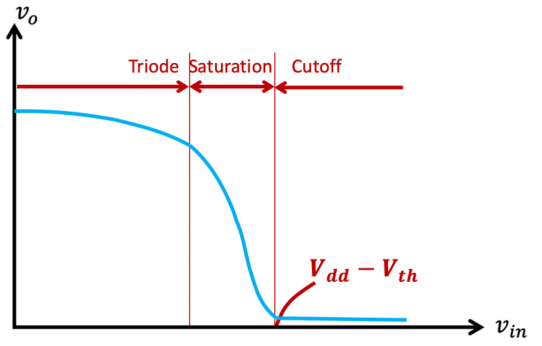
Connected to the most negative power supply to avoid body-effect

CMOS Inverter









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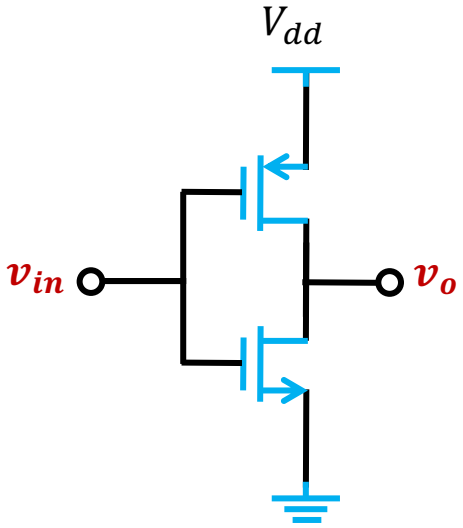
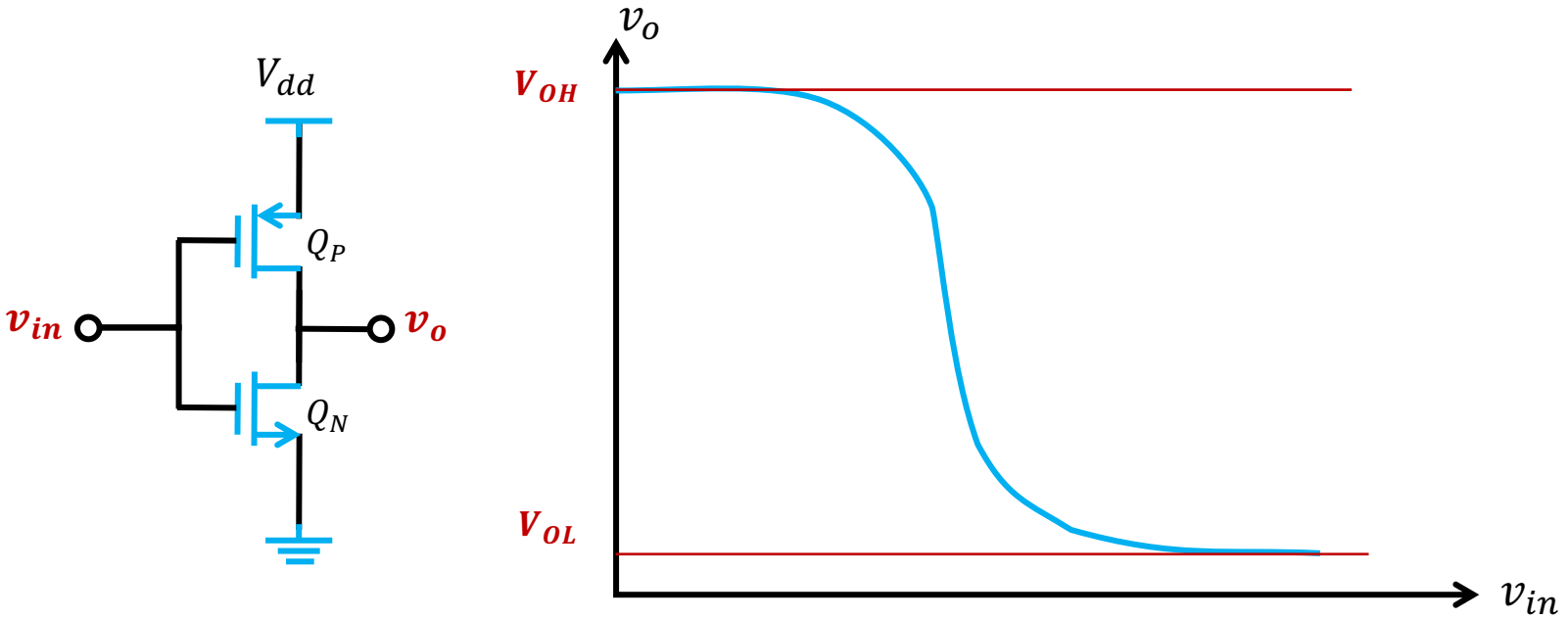
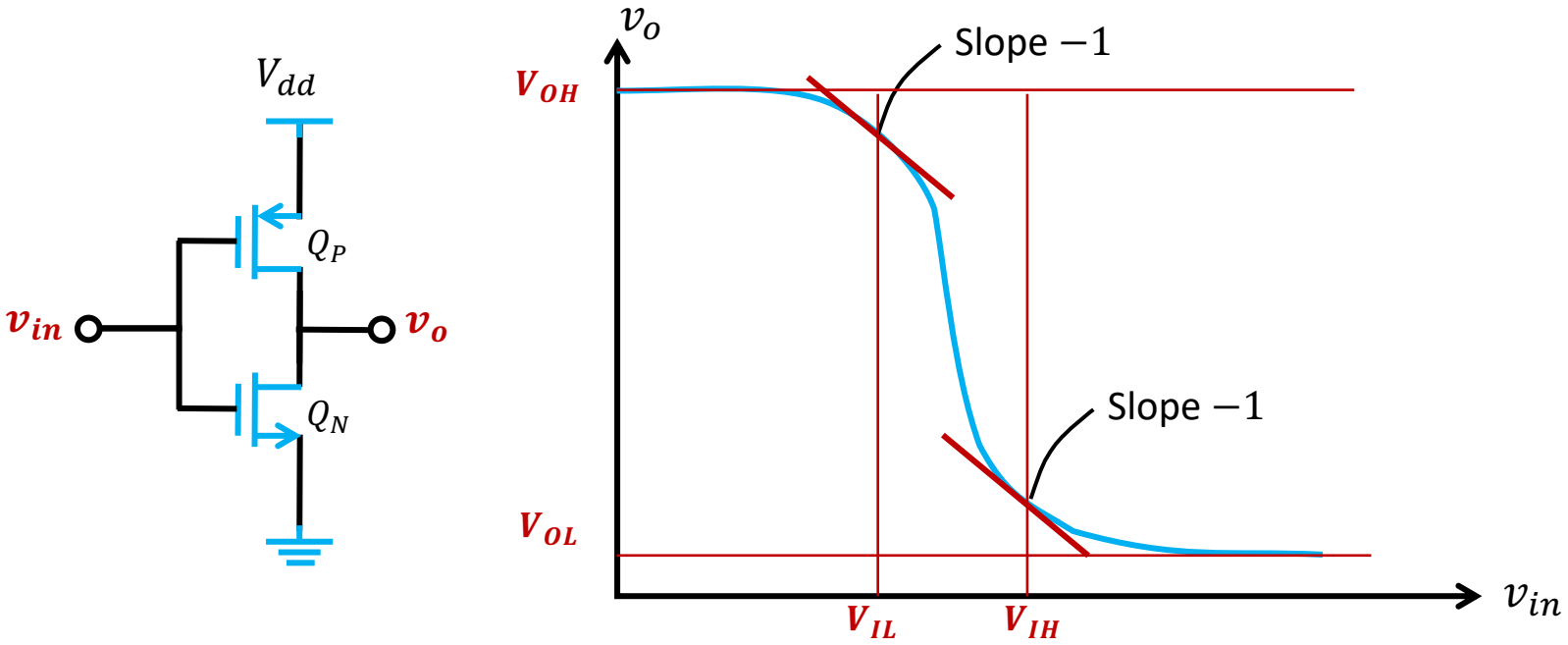


Voltage Transfer Characteristic (VTC)



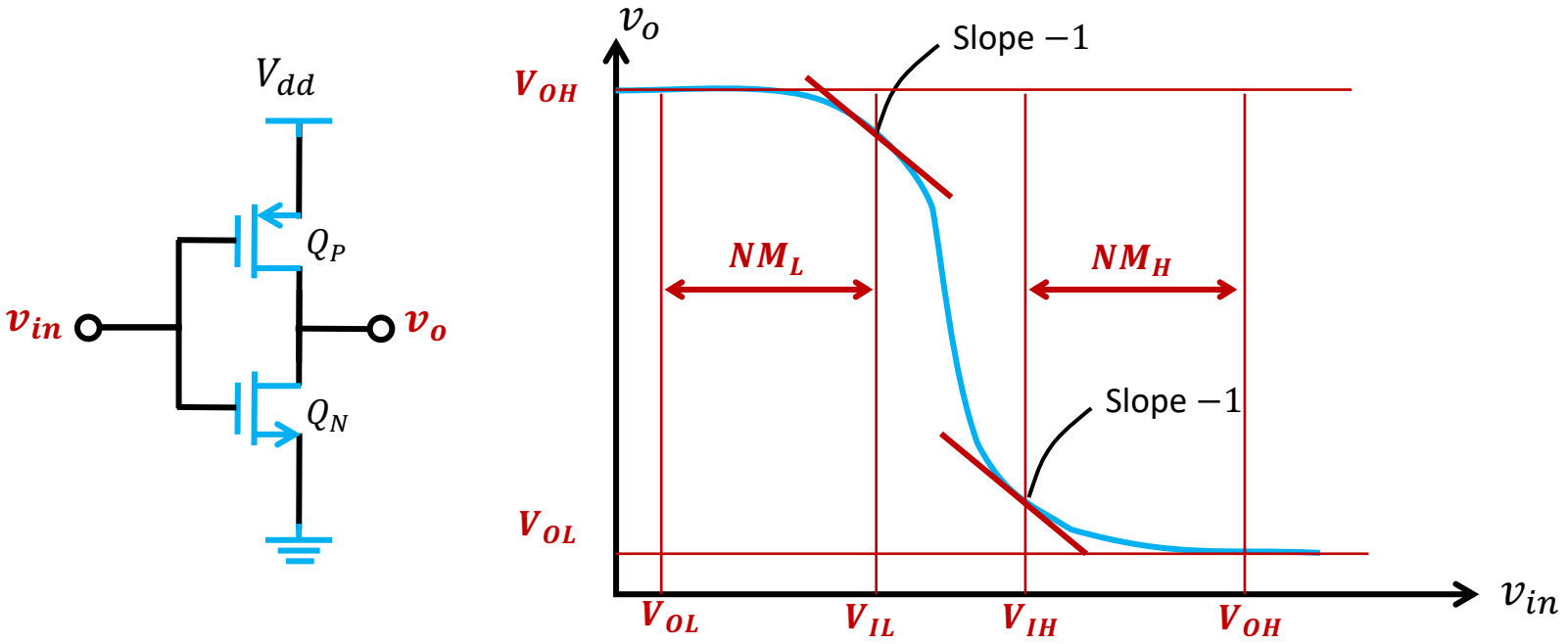
- Define OUTPUT HIGH LEVEL V_{OH} → Logic-1 output
- Define OUTPUT LOW LEVEL V_{OL} → Logic-0 output

Voltage Transfer Characteristic (VTC)



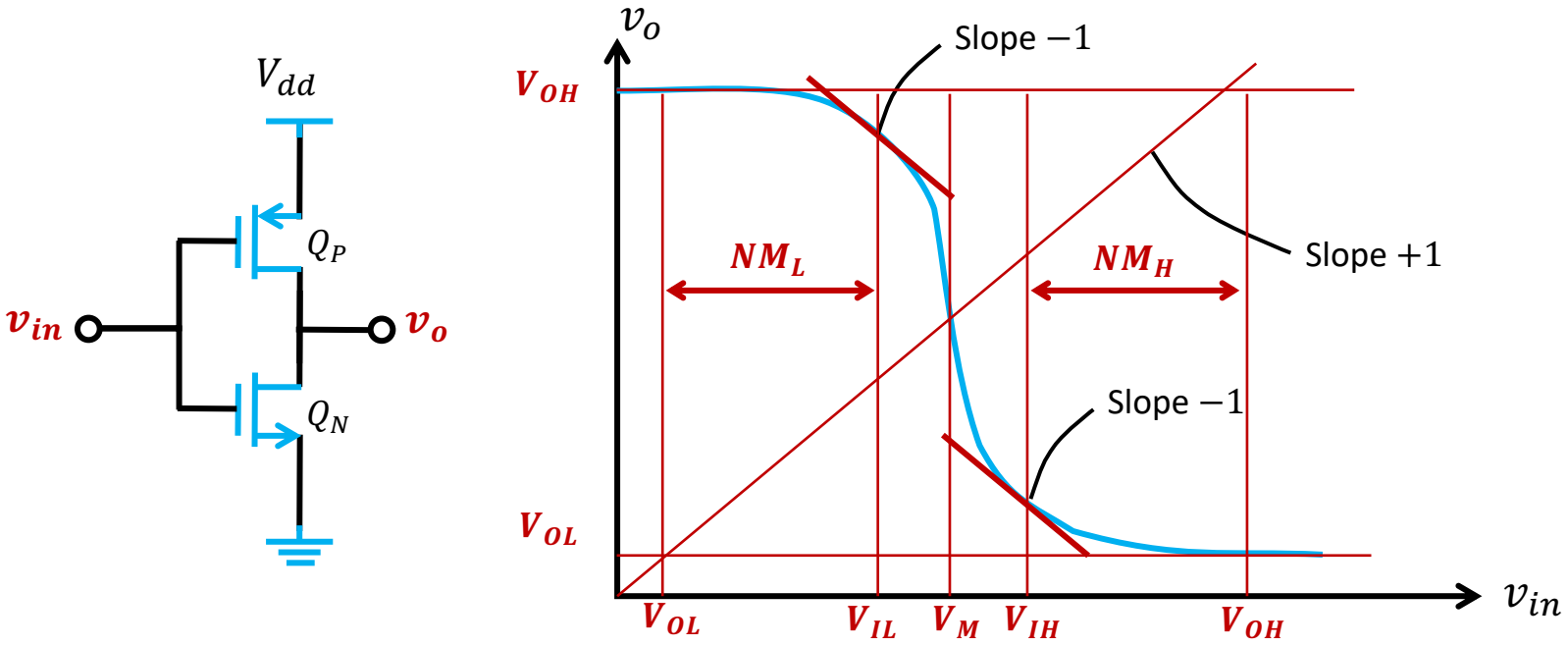
- **Define INPUT HIGH LEVEL V_{IH}** → **Minimum input to be presented as logic 1**
- **Define INPUT LOW LEVEL V_{IL}** → **Maximum input to be presented as logic 0**

Voltage Transfer Characteristic (VTC)



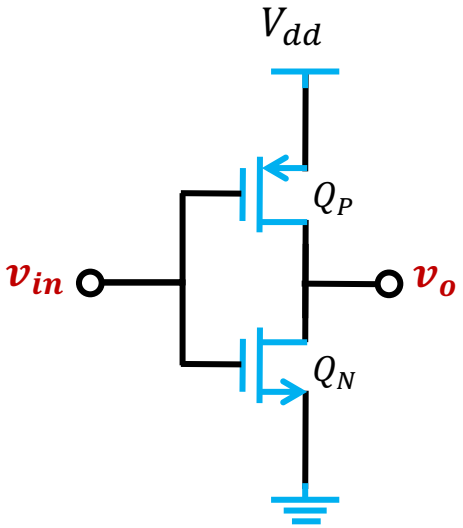
- **Define NOISE MARGIN FOR LOW INPUT** $NM_L = V_{IL} - V_{OL}$
- **Define NOISE MARGIN FOR HIGH INPUT** $NM_H = V_{OH} - V_{IH}$

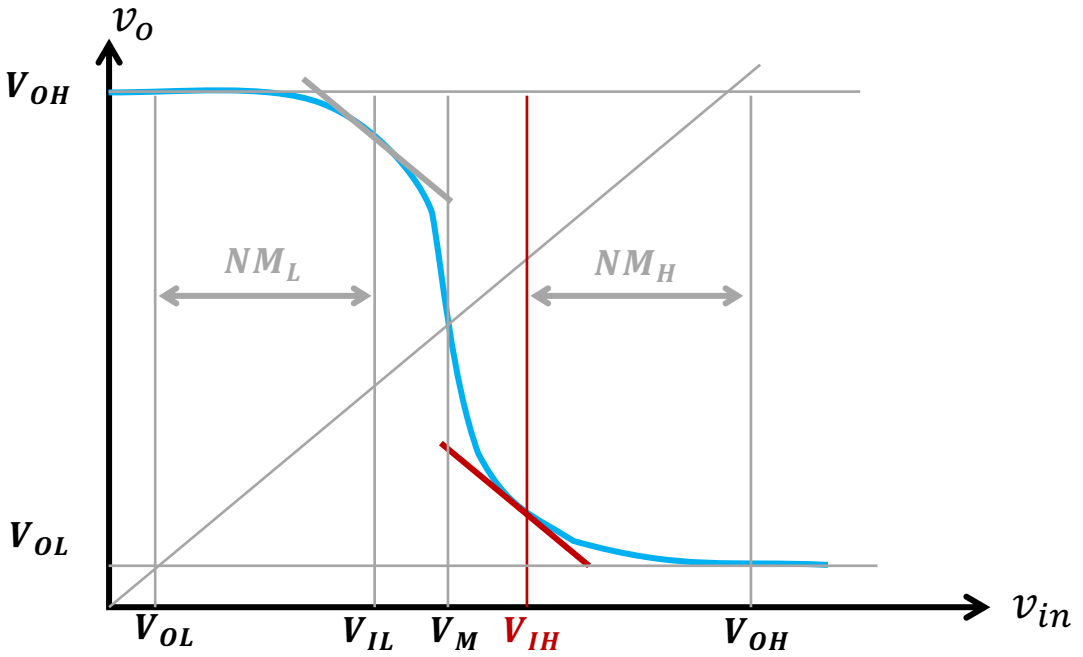
Voltage Transfer Characteristic (VTC)



- **Define midpoint of the VTC** $\quad V_M \xrightarrow{ideally} \frac{V_{dd}}{2}$

Voltage Transfer Characteristic (VTC)



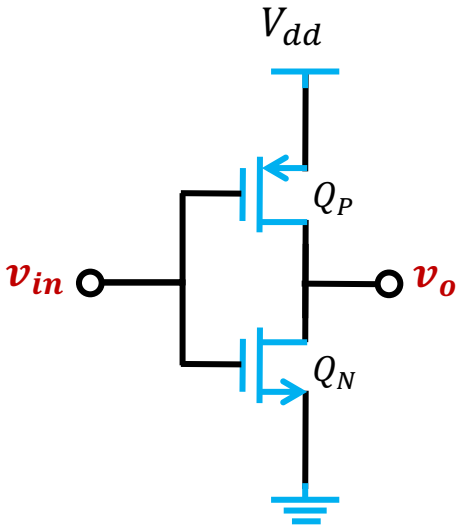


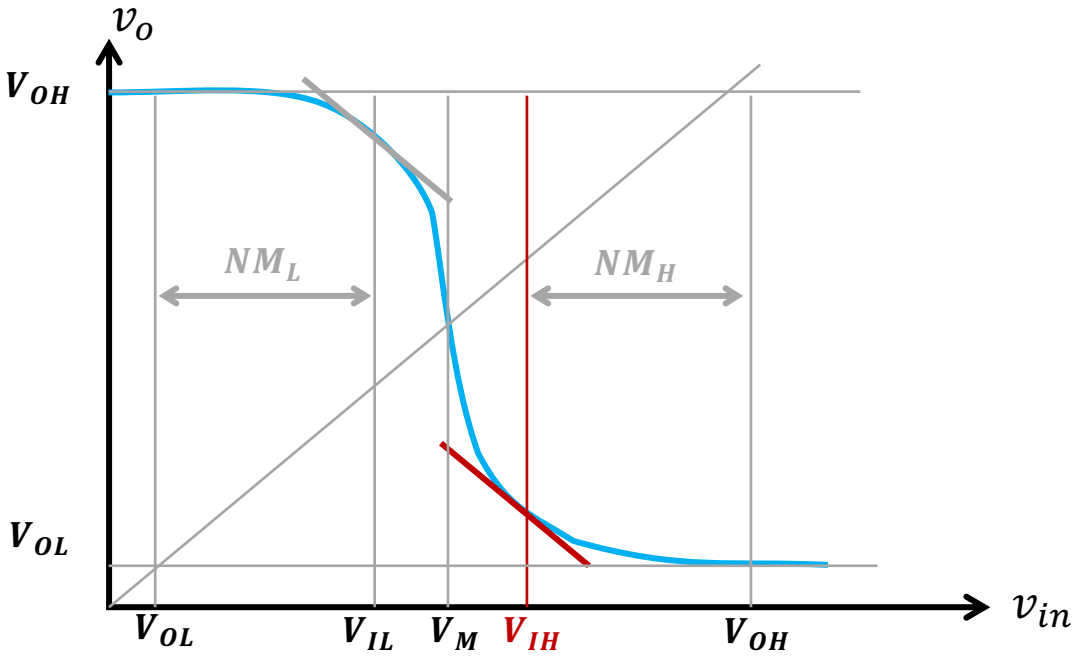
- **@ $v_{in} = V_{IH}$**

$$\begin{cases} v_{SG,P} \geq V_{th} \\ v_{DG,P} \leq V_{th} \end{cases} \Rightarrow \textbf{Q_P biased in Saturation region}$$

$$\begin{cases} v_{GS} \geq V_{th} \\ v_{GD} \geq V_{th} \end{cases} \Rightarrow \textbf{Q_N biased in Triode region}$$

Voltage Transfer Characteristic (VTC)





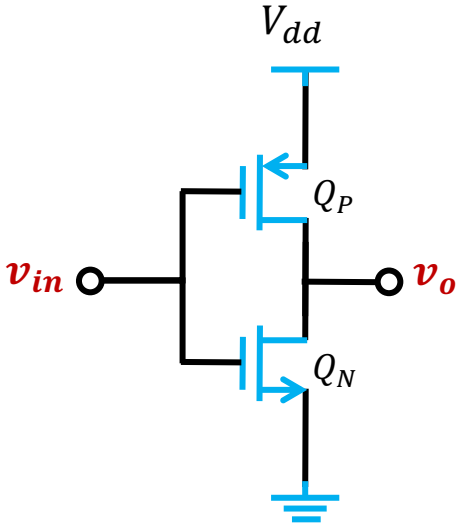
- $@\ v_{in} = V_{IH}$

$Q_P \in$ Saturation region

$Q_N \in$ Triode region

$$\begin{cases} i_{Dp} = i_{Dn} \\ i_{Dn} = (\mu_n C_{ox})\left(\frac{W}{L}\right)_n \left[(v_{GS,N} - V_{th})v_{DS,N} - \frac{1}{2}v_{DS,N}^2\right] \\ i_{Dp} = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)_p (|v_{GS,G}| - V_{th})^2 \end{cases}$$

Voltage Transfer Characteristic (VTC)



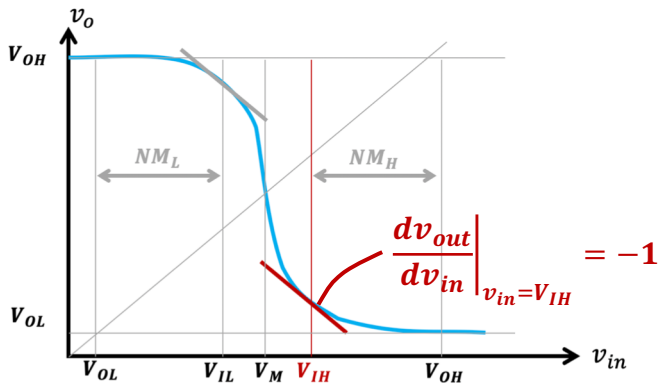
$$\begin{cases} i_{Dp} = i_{Dn} \\ i_{Dn} = (\mu_n C_{ox})\left(\frac{W}{L}\right)_n \left[(v_{GS,N} - V_{th})v_{DS,N} - \frac{1}{2}v_{DS,N}^2\right] \\ i_{Dp} = \frac{1}{2}(\mu_p C_{ox})\left(\frac{W}{L}\right)_p (|v_{GS,G}| - V_{th})^2 \end{cases}$$

Assume $(\mu_n C_{ox})\left(\frac{W}{L}\right)_n = (\mu_p C_{ox})\left(\frac{W}{L}\right)_p$

$$(v_{in} - V_{th})v_{out} - \frac{1}{2}v_{out}^2 = \frac{1}{2}(V_{dd} - v_{in} - V_{th})^2$$

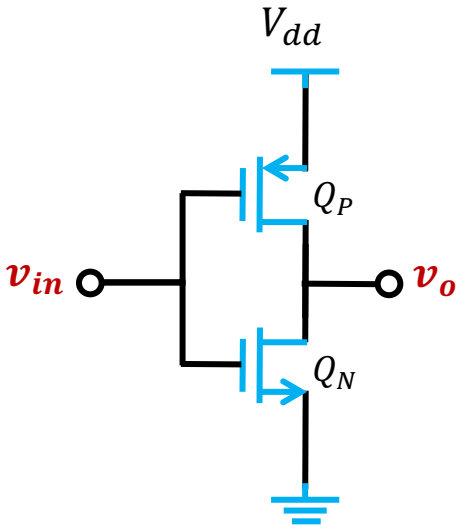
$$(v_{in} - V_{th})\frac{dv_{out}}{dv_{in}} + v_{out} - v_{out}\frac{dv_{out}}{dv_{in}} = -(V_{dd} - v_{in} - V_{th})$$

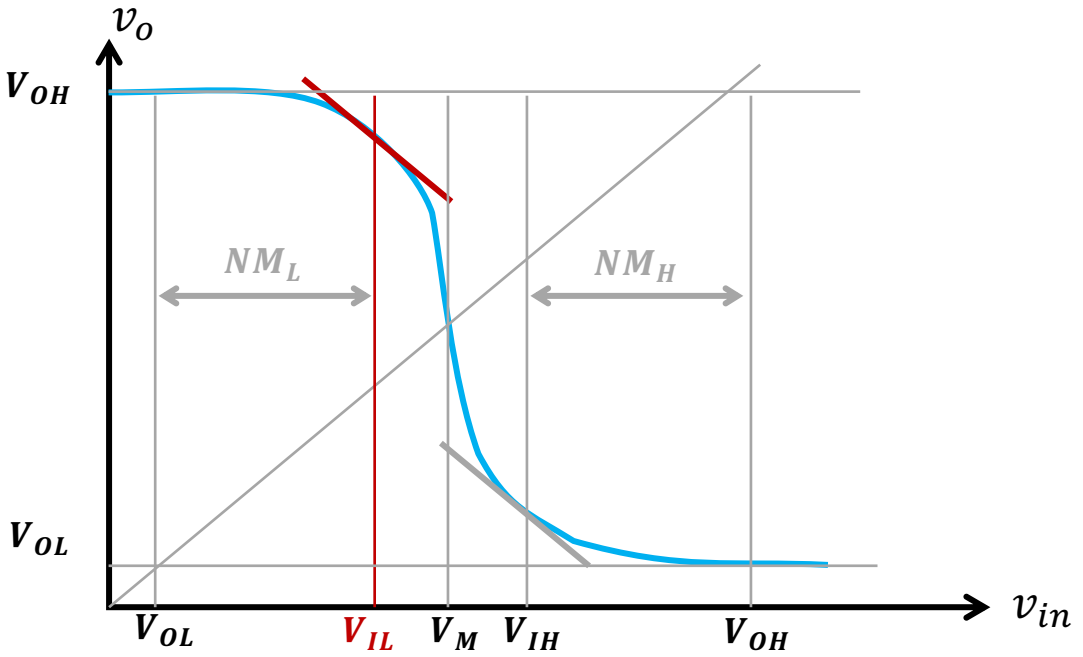
$$v_{out} = -\frac{V_{dd}}{2} + v_{in}$$



$$V_{IH} = \frac{5V_{dd} - 2V_{th}}{8}$$

Voltage Transfer Characteristic (VTC)



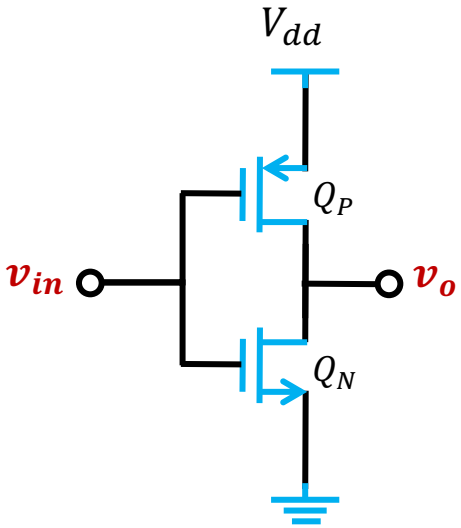


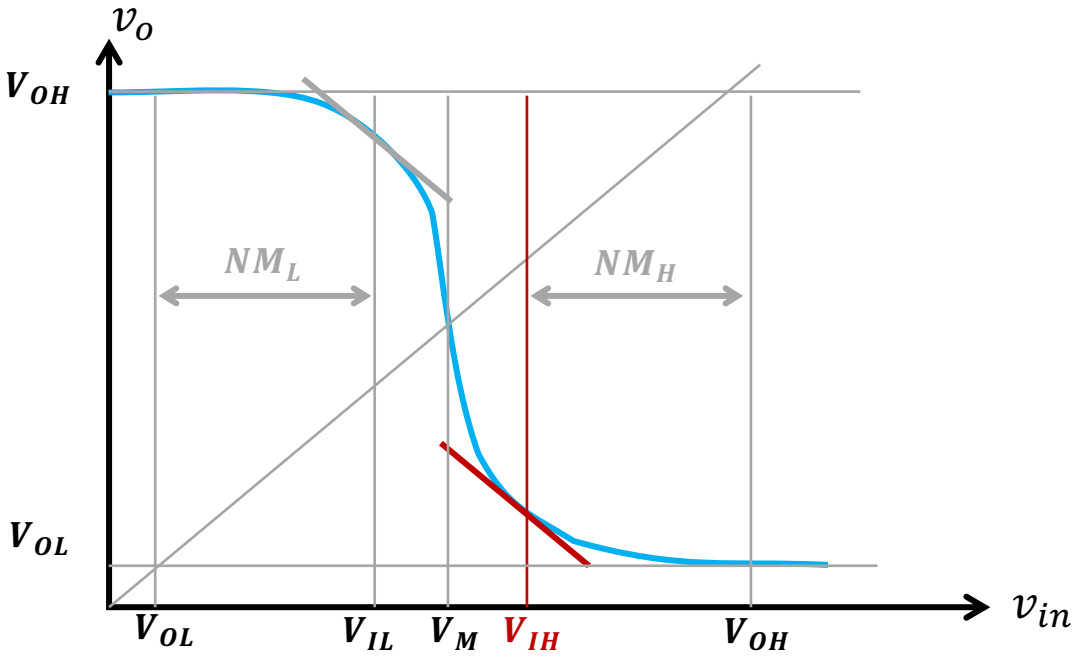
- **@ $v_{in} = V_{IL}$**

$$\begin{cases} v_{SG,P} \geq V_{th} \\ v_{DG,P} \geq V_{th} \end{cases} \Rightarrow \text{**Q_P biased in Triode region**}$$

$$\begin{cases} v_{GS} \geq V_{th} \\ v_{GD} \leq V_{th} \end{cases} \Rightarrow \text{**Q_N biased in Saturation region**}$$

Voltage Transfer Characteristic (VTC)





- **@ $v_{in} = V_{IL}$**

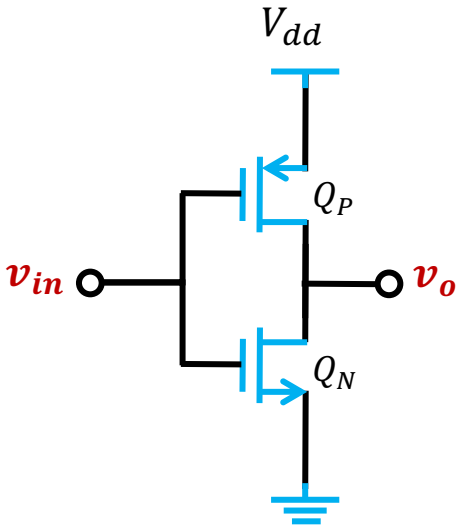
Q_P ∈ Triode region

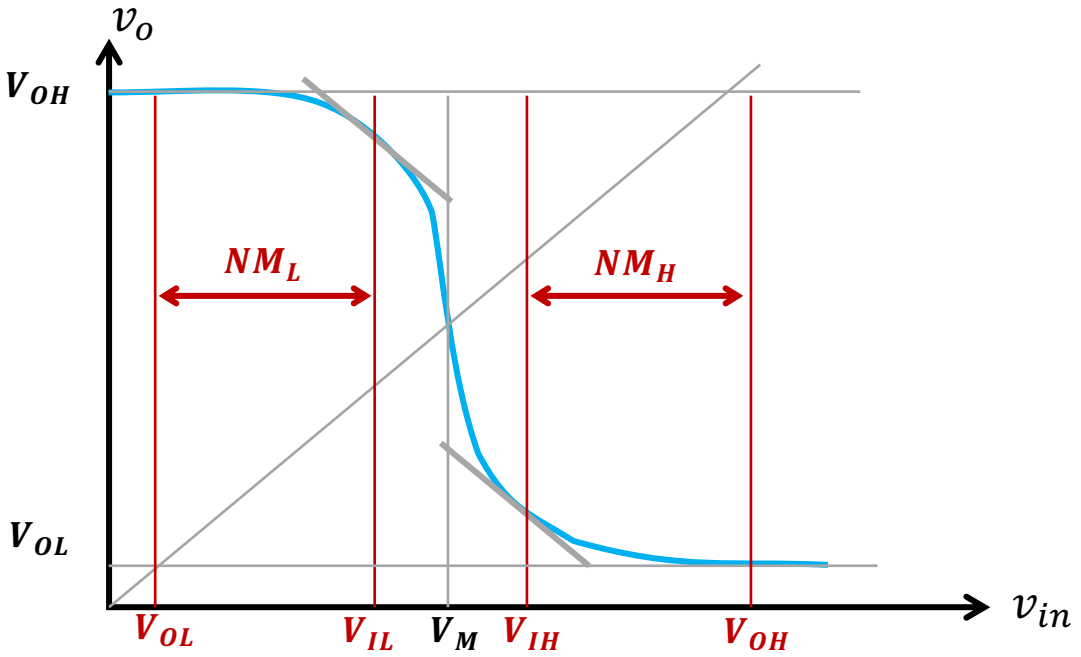
Q_N ∈ Saturation region

- Similarly as @ $v_{in} = V_{IH}$

$$V_{IL} = \frac{3V_{dd} + 2V_{th}}{8}$$

Voltage Transfer Characteristic (VTC)





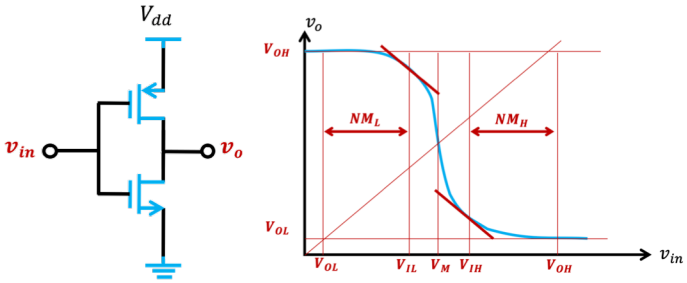
$$\begin{cases} V_{IH} = \dfrac{5V_{dd} - 2V_{th}}{8} \\ V_{IL} = \dfrac{3V_{dd} + 2V_{th}}{8} \end{cases}$$

$$NM_L = V_{IL} - \underbrace{V_{OL}}_{0} = \frac{3V_{dd} + 2V_{th}}{8}$$

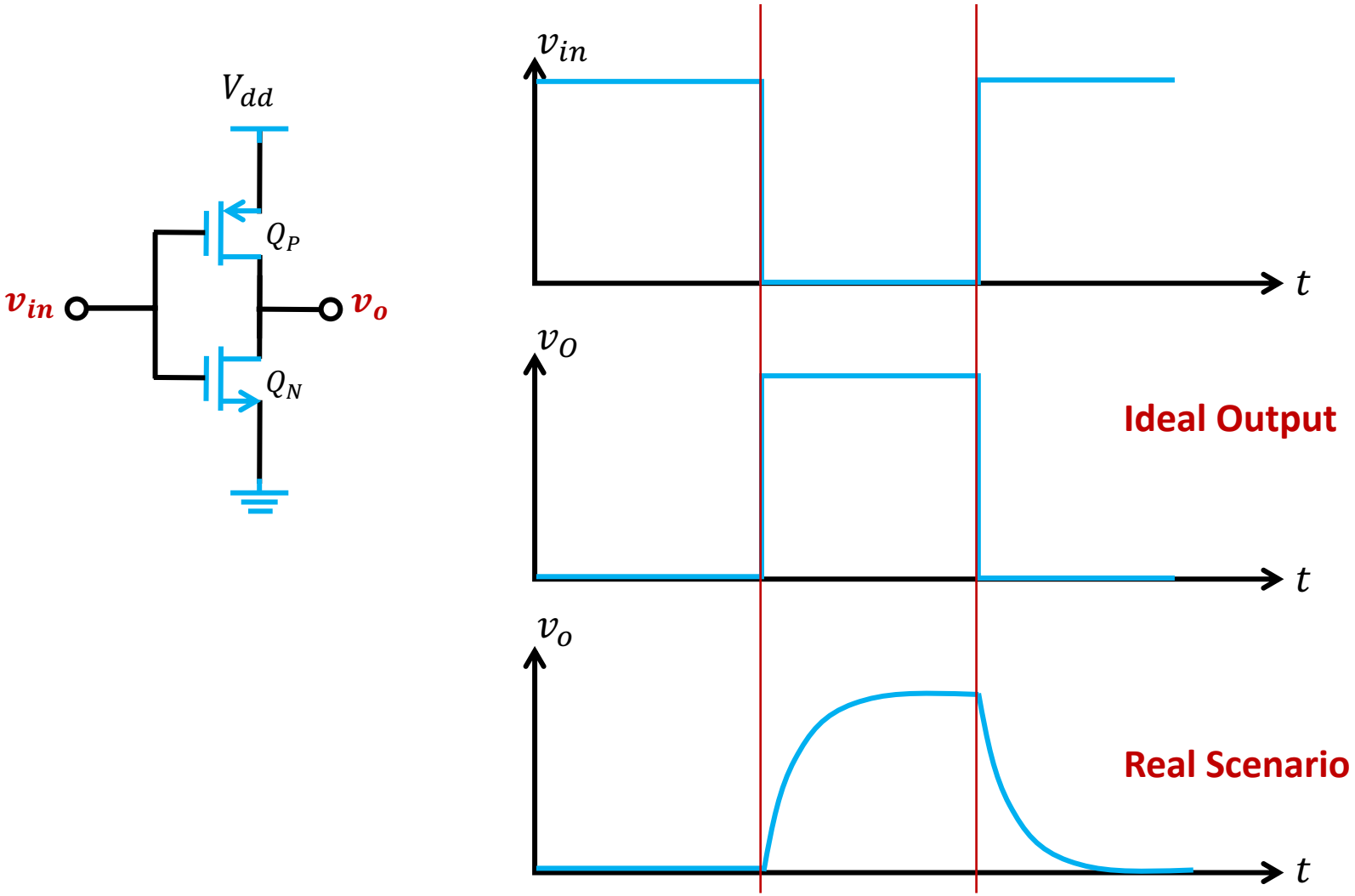
$$NM_H = \underbrace{V_{OH}}_{V_{dd}} - V_{IH} = \frac{3V_{dd} + 2V_{th}}{8}$$

Outline

- CMOS Inverters
  - Voltage Transfer Characteristic (VTC)
  - Noise margin
  - **Propagation delay**

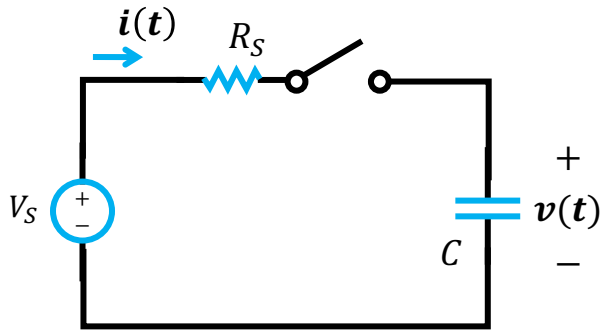


Propagation delay



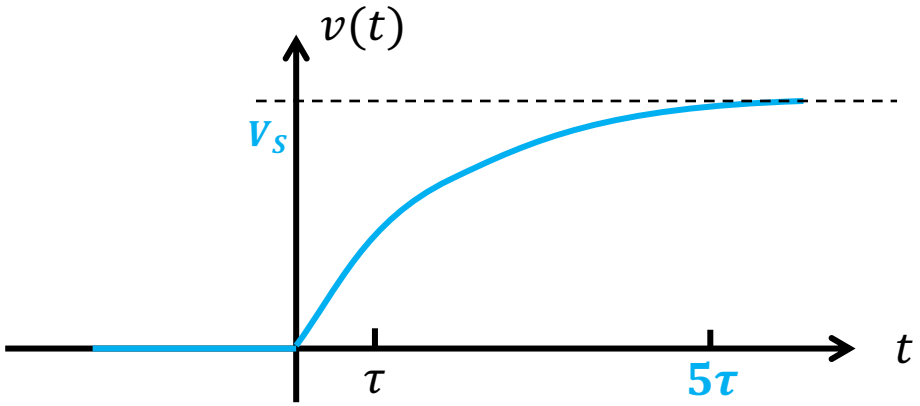
Recall: charging of a capacitor

QUESTION: Assume there is no charge on the capacitor C before the switch is turned on. Find the response after the switch is turned on.

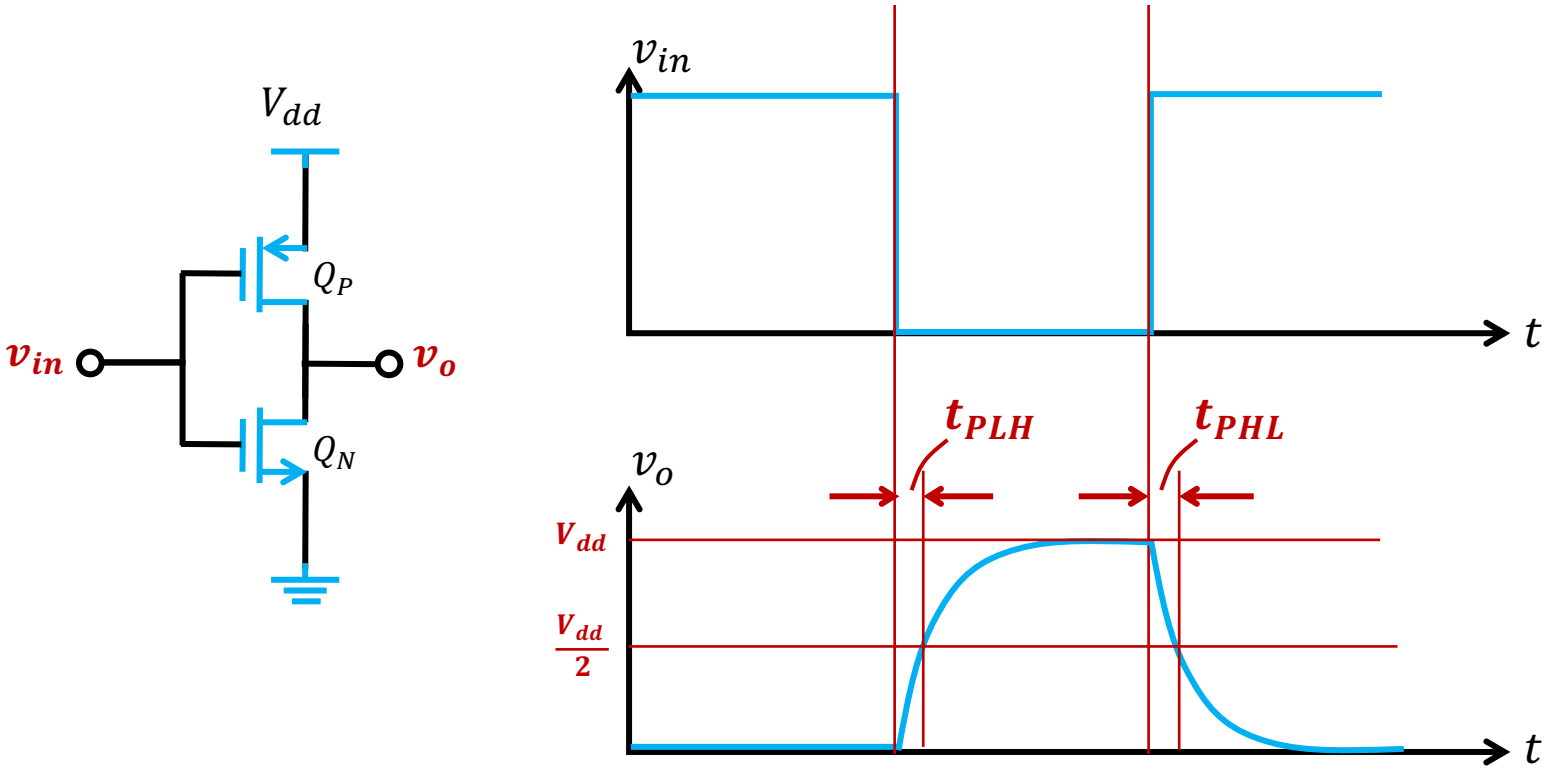


$$\frac{d}{dt}v(t) + \frac{1}{RC}v(t) = \frac{1}{RC}V_S$$

Solution: $v(t) = V_S - V_S e^{-\frac{1}{RC}t}$

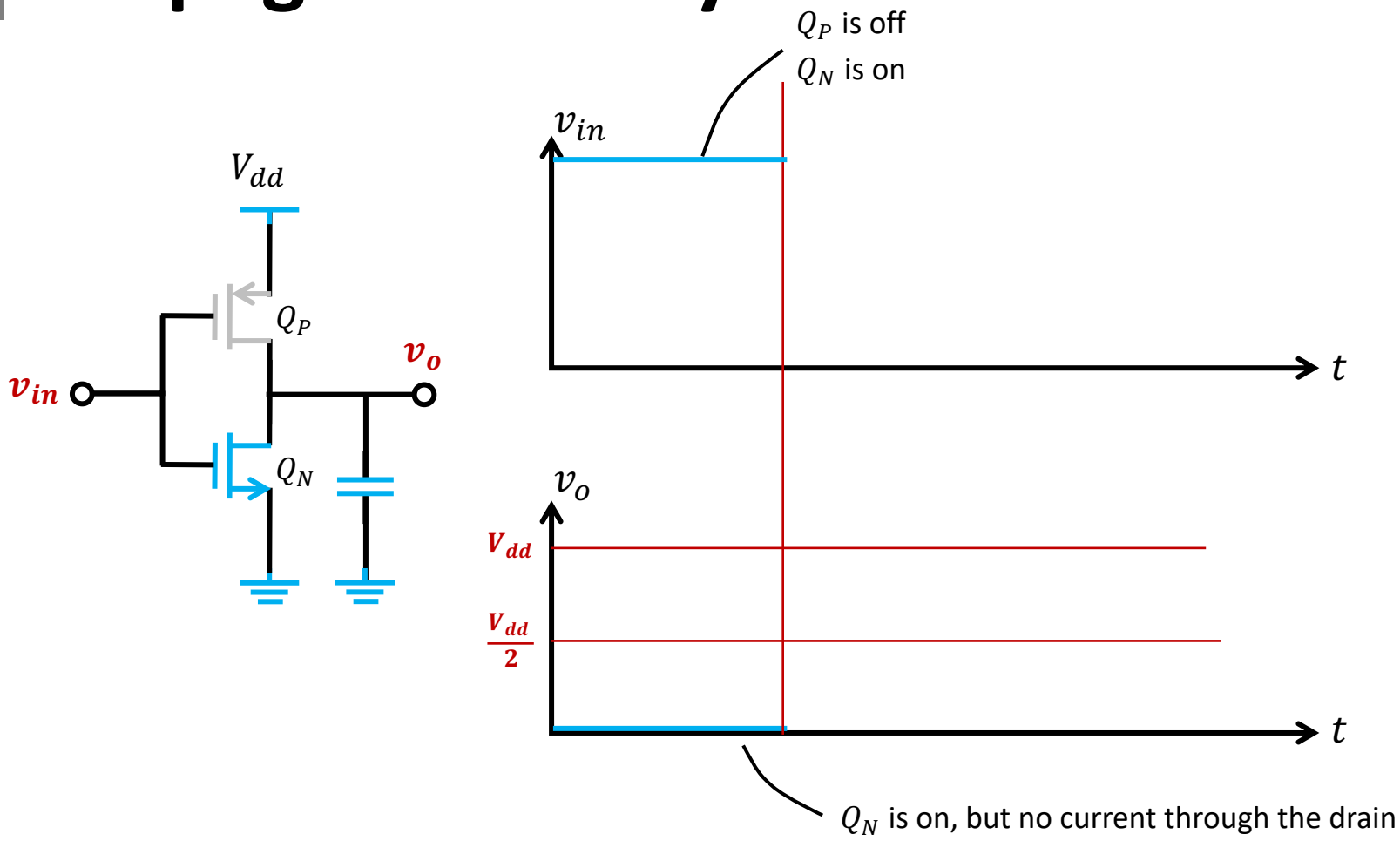


Propagation delay

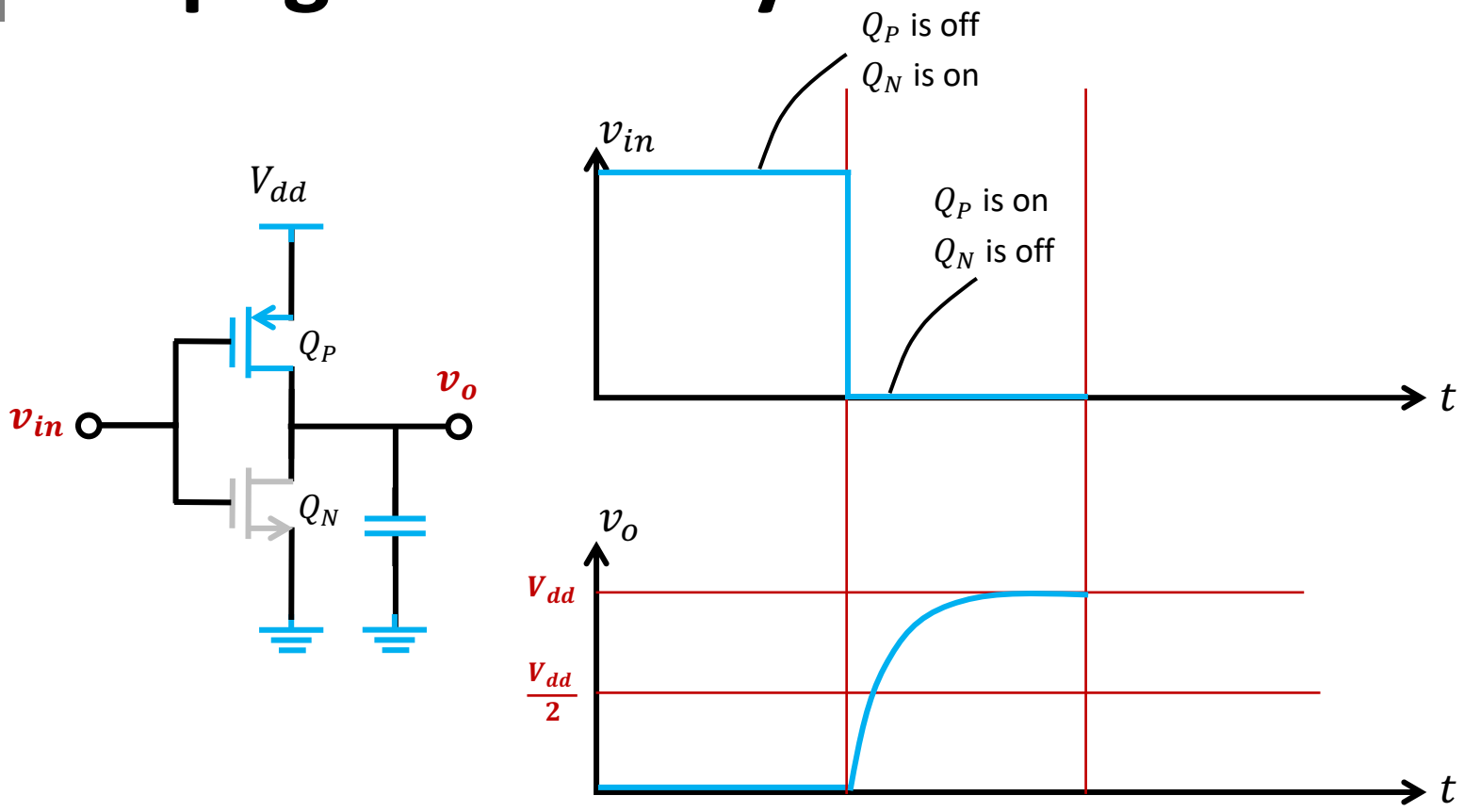


- **Propagation delay for the output from LOW to HIGH** t_{PLH}
- **Propagation delay for the output from HIGH to LOW** t_{PHL}

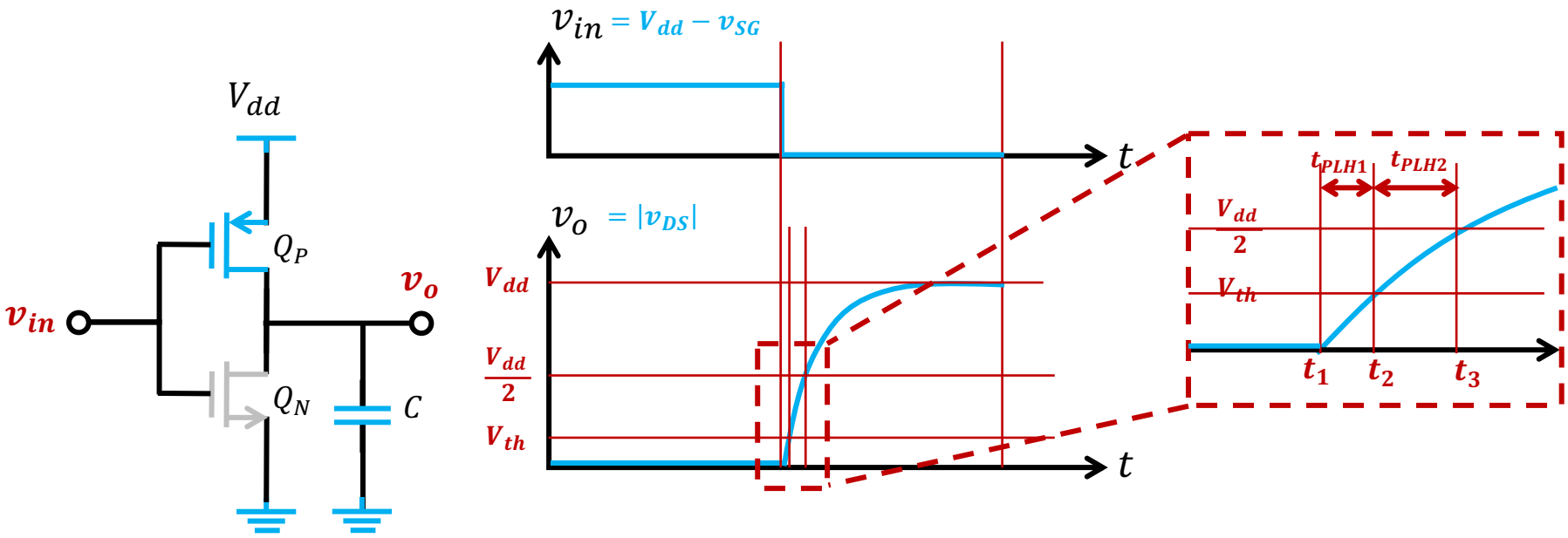
Propagation delay



Propagation delay



Propagation delay

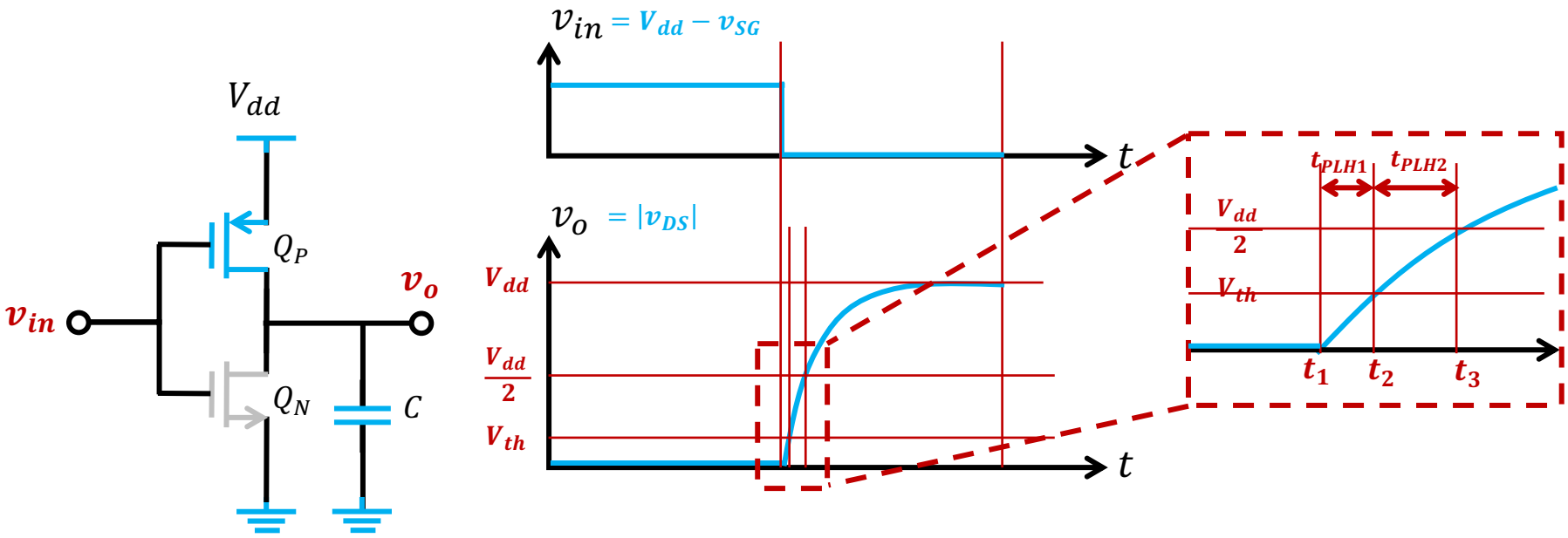


- While $t \in [t_1^+, t_2]$

$$\begin{cases} v_{SG} = V_{dd} \geq V_{th} \\ v_{DG} = v_o \leq V_{th} \end{cases}$$

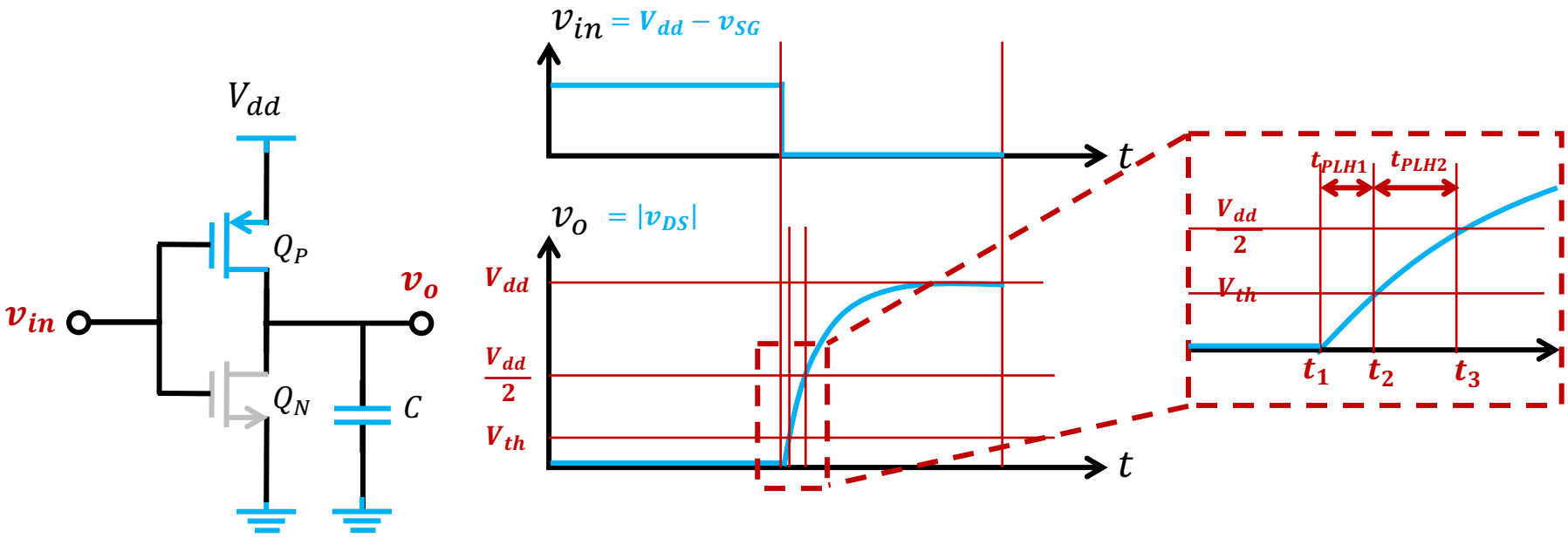
Q_P biased in Saturation region

Propagation delay



- While $t \in [t_1^+, t_2]$ $\quad Q_P \in$ **Saturation region**
- The drain current $\quad i_{D1} = \frac{1}{2} k_p (|v_{GS}| - V_{th})^2$
- The delay $\quad t_{PLH1} = t_2 - t_1 = C\frac{\Delta v_{out}}{i_D} = C\frac{V_{th}}{i_{D1}} = 2C\frac{V_{th}}{k_p(V_{dd} - V_{th})^2}$

Propagation delay

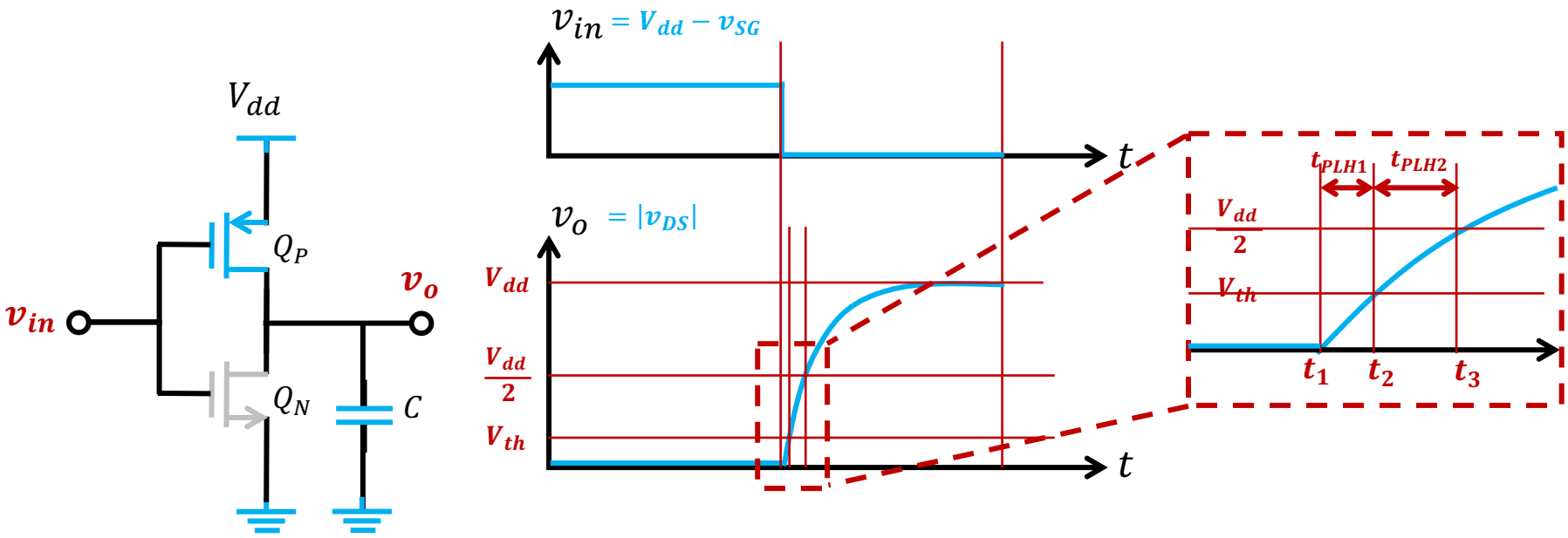


- While $t \in [t_2^+, t_3]$

$$\begin{cases} v_{SG} = V_{dd} \geq V_{th} \\ v_{DG} = v_o > V_{th} \end{cases}$$

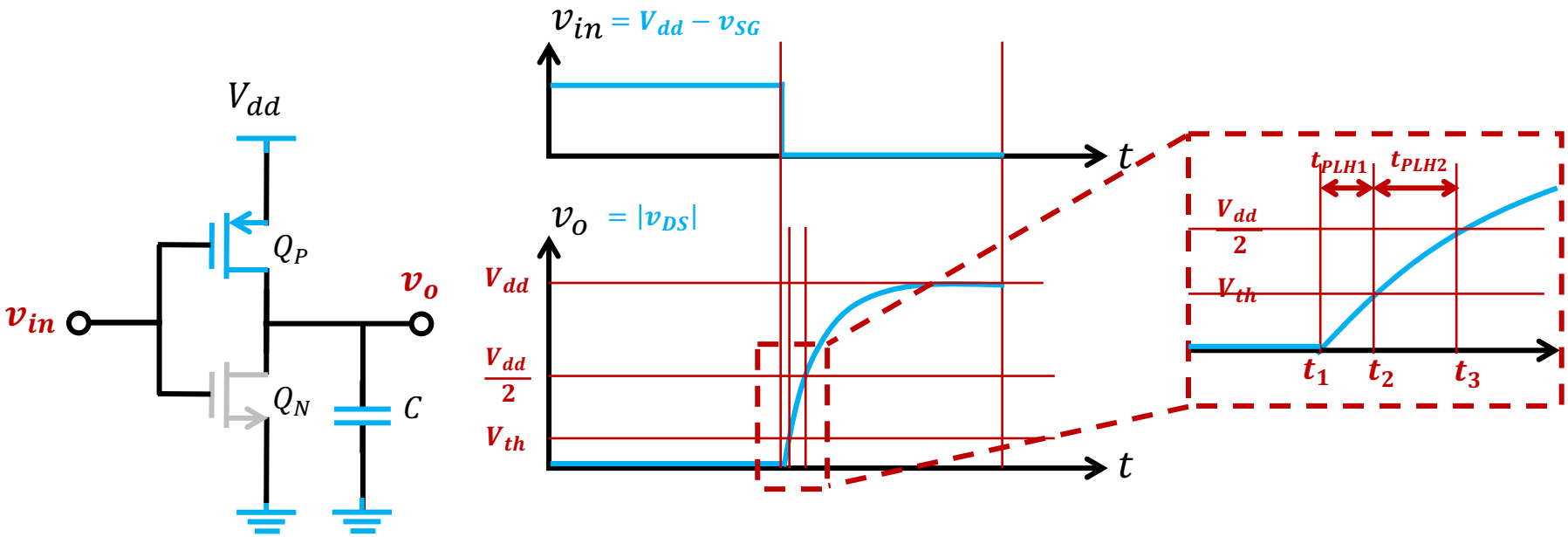
Q_P biased in triode region

Propagation delay



- While $t \in [t_2^+, t_3]$ $\quad Q_P \in$ **Triode region**
- The drain current $\quad i_{D2} = k_p\left[(|v_{GS}| - V_{th})|v_{DS}| - \frac{1}{2}v_{DS}^2\right]$
- The delay $\quad t_{PLH1} = \int_{t_2}^{t_3} C\frac{dv_o}{di_{D2}} = \frac{C}{k_p}\int_{V_{th}}^{\frac{V_{dd}}{2}} \frac{1}{(V_{dd} - V_{th})(V_{dd} - v_o) - \frac{1}{2}(V_{dd} - v_o)^2} dv_o$

Propagation delay



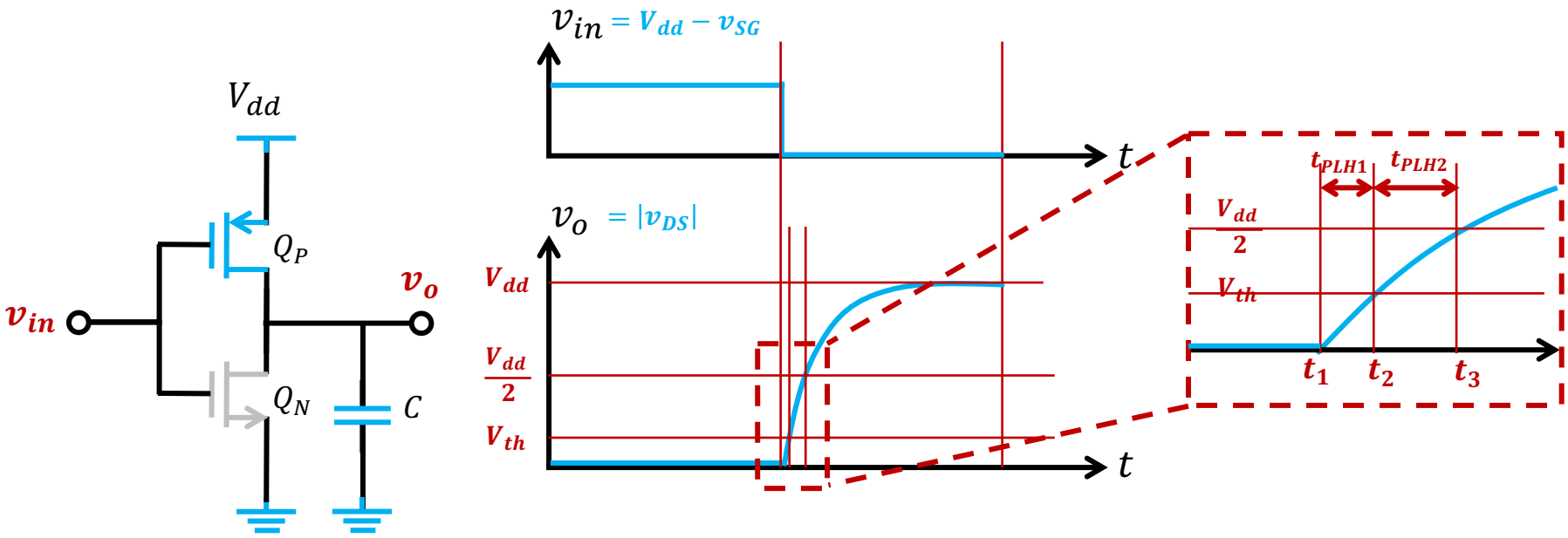
- The delay

$$t_{PLH1} = \frac{C}{k_p}\int_{V_{th}}^{\frac{V_{dd}}{2}} \frac{1}{(V_{dd} - V_{th})(V_{dd} - v_o) - \frac{1}{2}(V_{dd} - v_o)^2} dv_o$$

$$= \frac{C}{k_p(V_{dd} - V_{th})} In\left(\frac{2(V_{dd} - V_{th}) - (V_{dd} - v_o)}{V_{dd} - v_o}\right)\Bigg|_{V_{th}}^{\frac{V_{dd}}{2}}$$

$$= \frac{C}{k_p(V_{dd} - V_{th})} In\left(\frac{3V_{dd} - 4V_{th}}{V_{dd}}\right)$$

Propagation delay



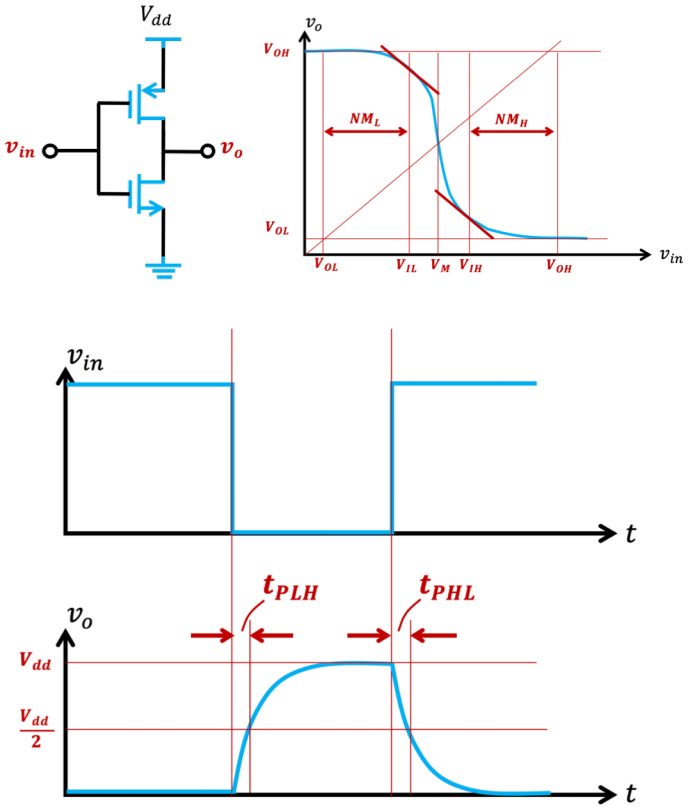
- The total delay $\boldsymbol{t_{PLH} = t_{PLH1} + t_{PLH2}}$

$$= 2C\frac{V_{th}}{k_p(V_{dd} - V_{th})^2} + \frac{C}{k_p(V_{dd} - V_{th})} In\left(\frac{3V_{dd} - 4V_{th}}{V_{dd}}\right)$$

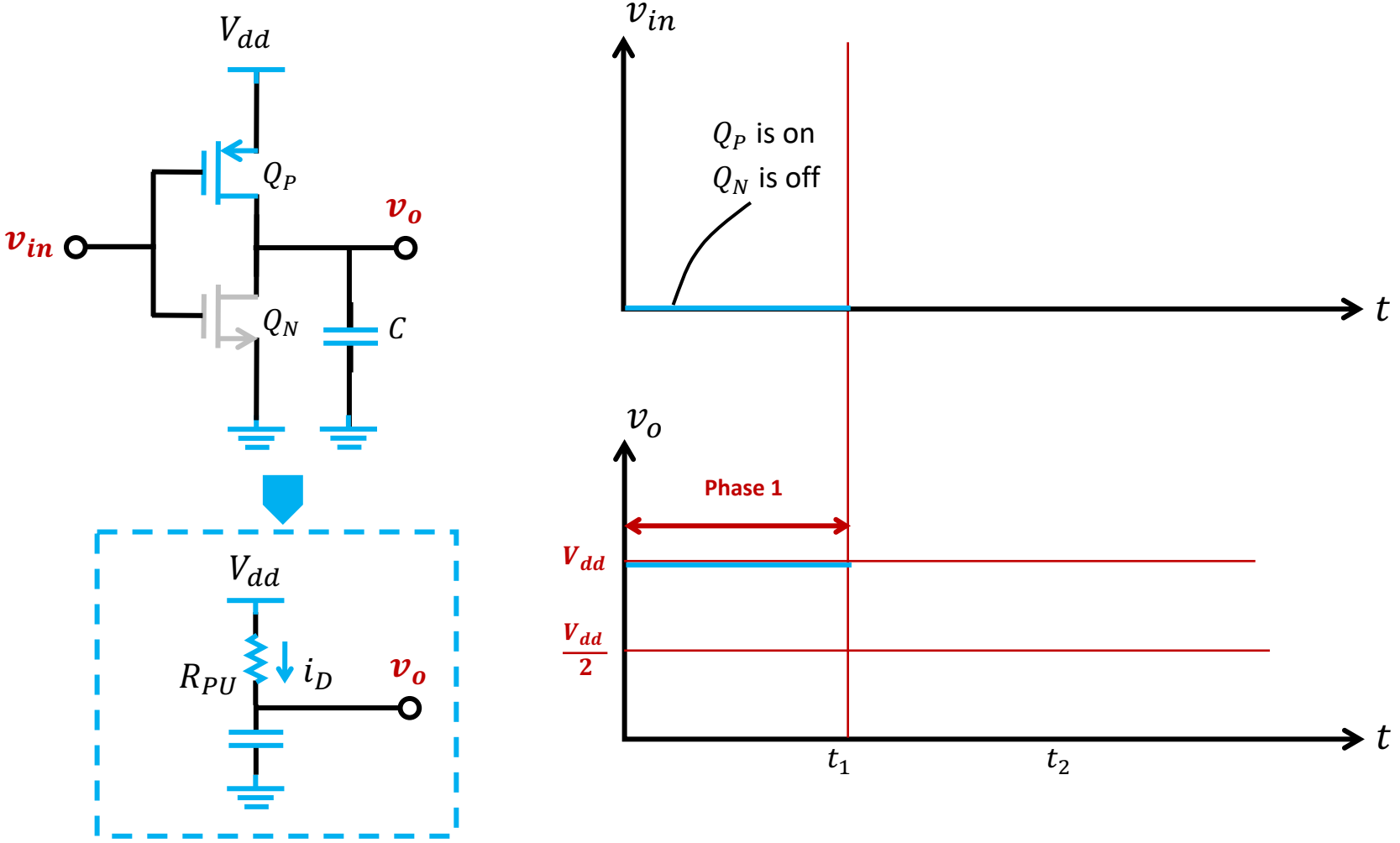
- Typically $V_{th} = 0.2V_{dd}$ ⇒ $\boldsymbol{t_{PLH} \approx \frac{1.6C}{k_p V_{dd}}}$

Outline

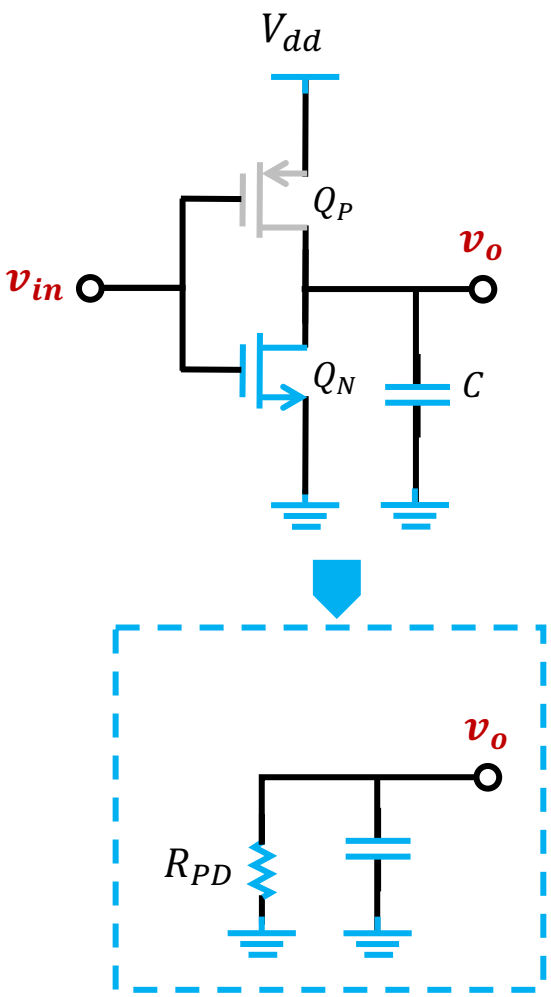
- CMOS Inverters
  - Voltage Transfer Characteristic (VTC)
  - Noise margin
  - Propagation delay
  - **Power consumption**

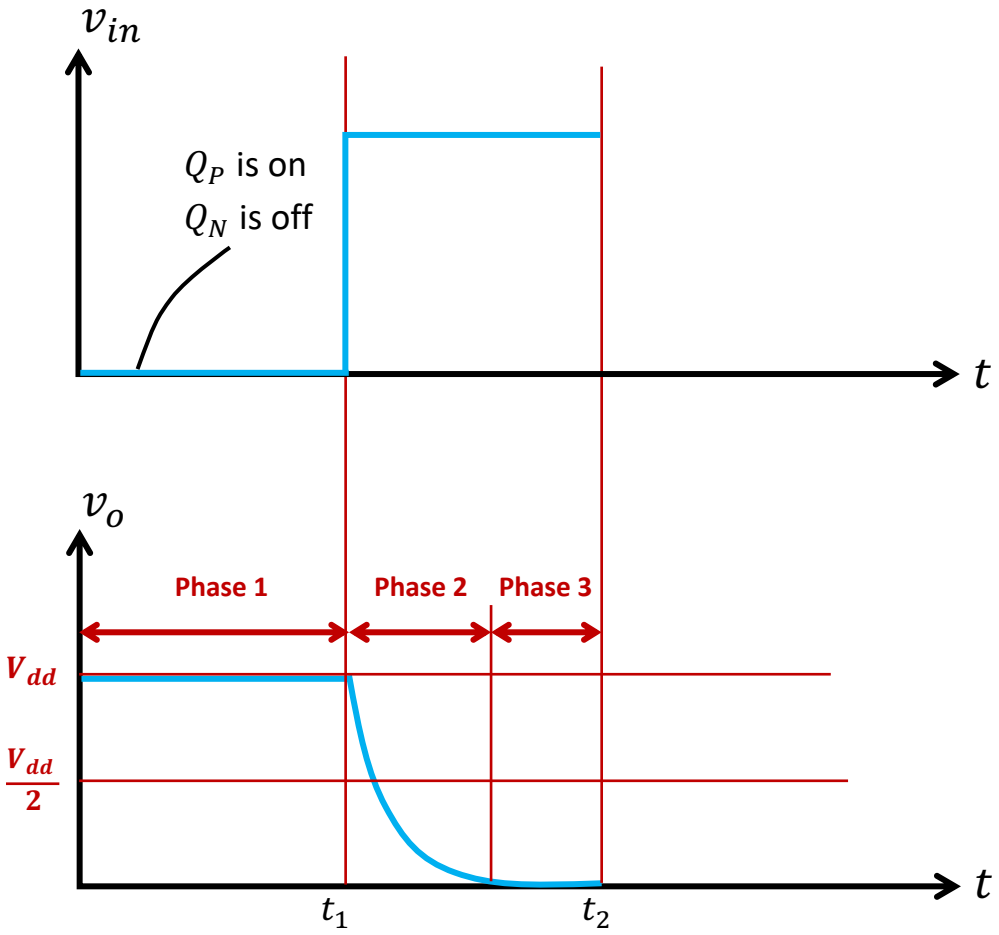


Power Consumption

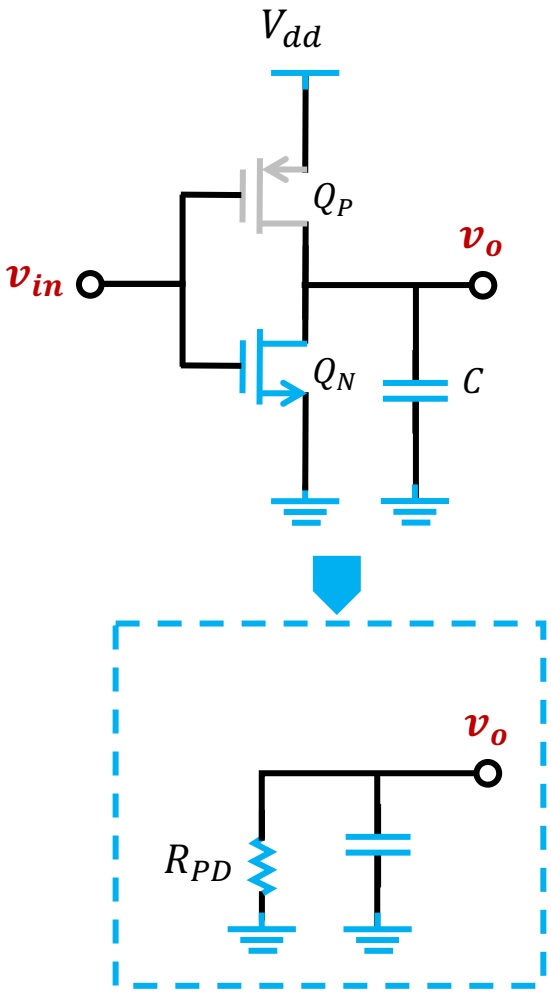


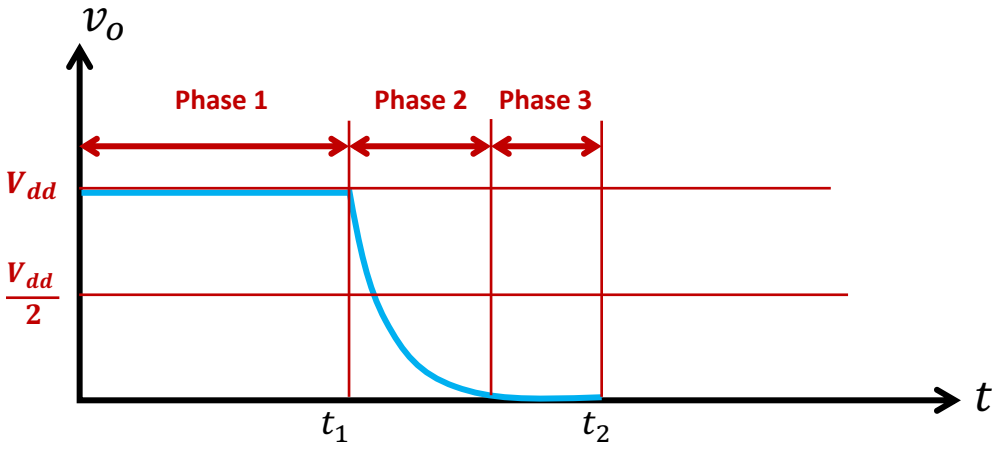
Power Consumption





Power Consumption

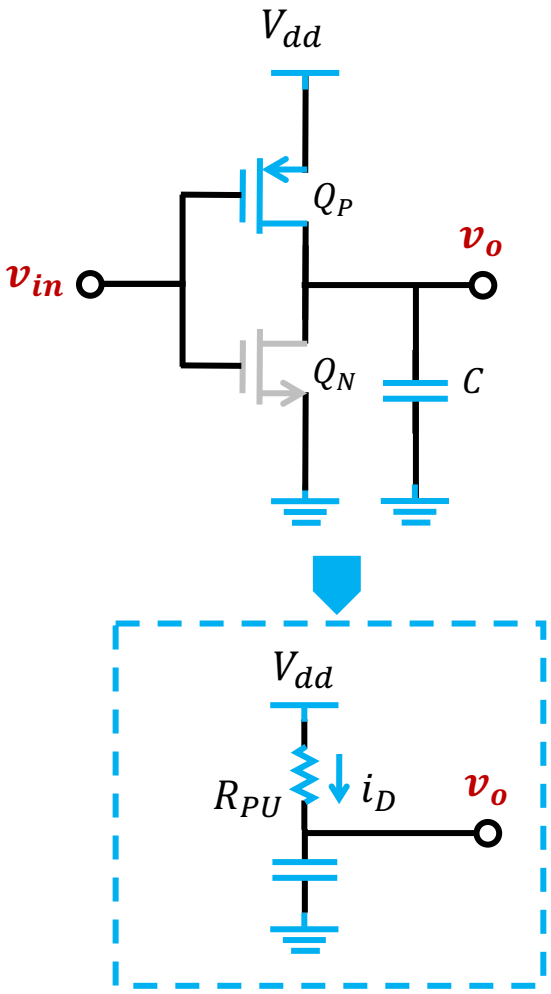


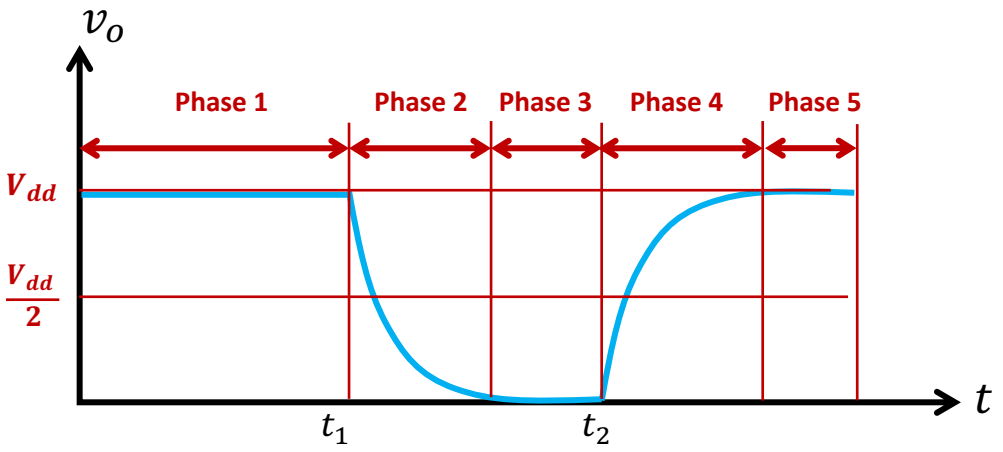


- @ Phase 1, energy stored in C is $E_{stored} = \frac{1}{2}CV_{dd}^2$
- @ Phase 3, NO energy left
- Thus, energy dissipated in R_{PD} @Phase 2 is

$$E_{dissipated} = \frac{1}{2}CV_{dd}^2$$

Power Consumption



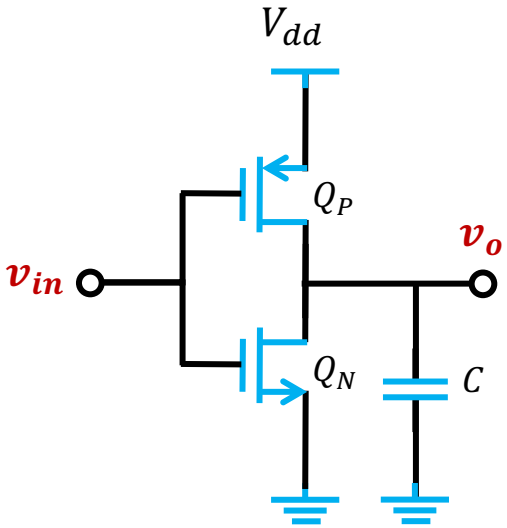


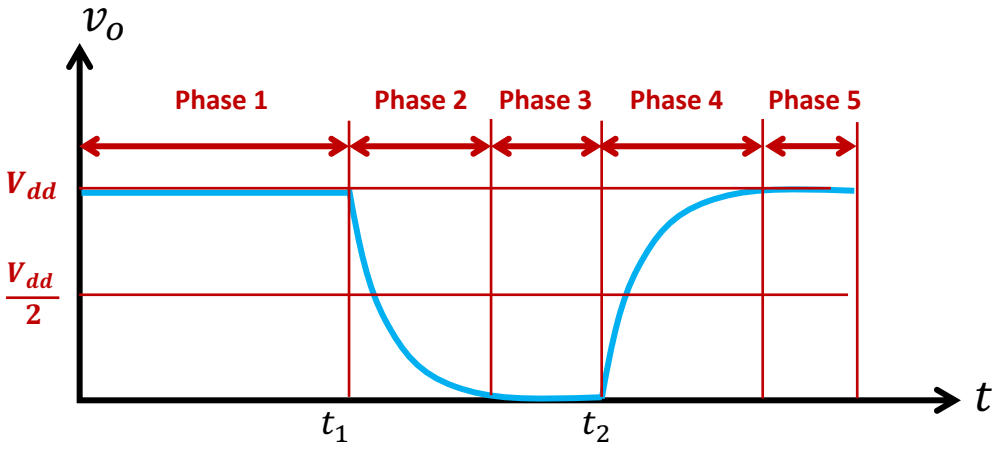
- @ Phase 4, energy provided by the power

$$E_{V_{dd}} = \int V_{dd} i dt = V_{dd} \int i dt = V_{dd} \mathrm{Q} = C V_{dd}^2$$

- @ Phase 5, energy stored in C is $E_{stored} = \frac{1}{2} C V_{dd}^2$
- Energy dissipated in R_{PU} is $E_{dissipated} = \frac{1}{2} C V_{dd}^2$

Power Consumption





- Total dissipated energy per cycle

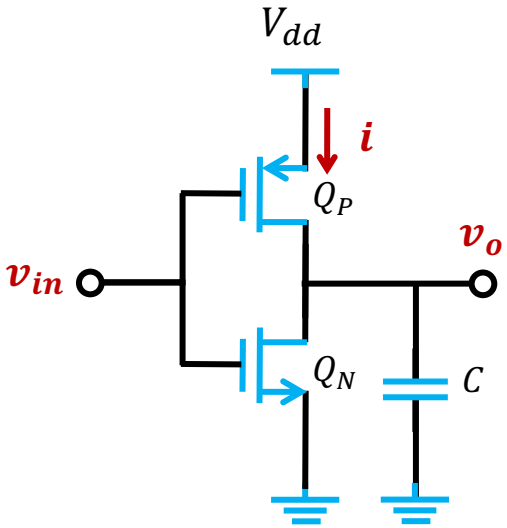
$$E_{dissipated} = CV_{dd}^2$$

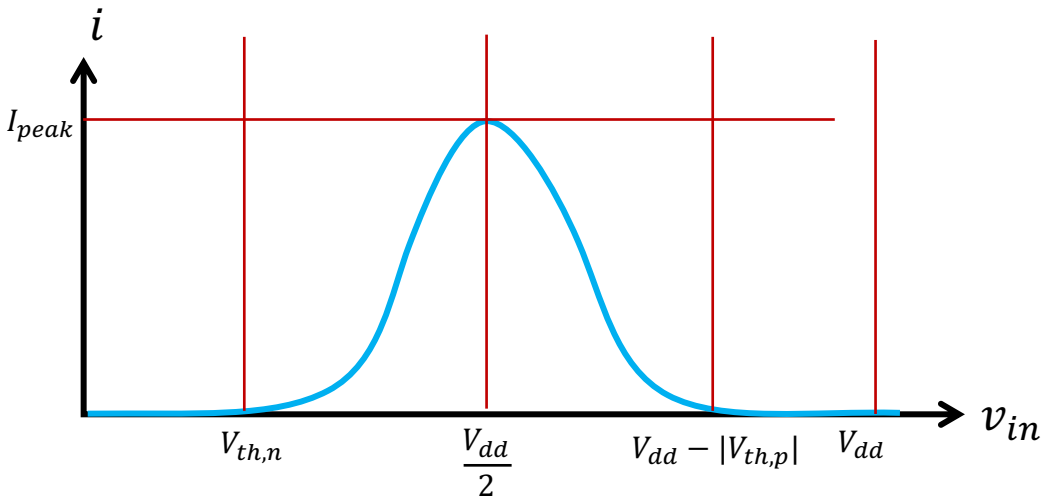
- The dynamic power dissipation

$$P_{dyn} = fCV_{dd}^2$$

inverter switch frequency

Power Consumption



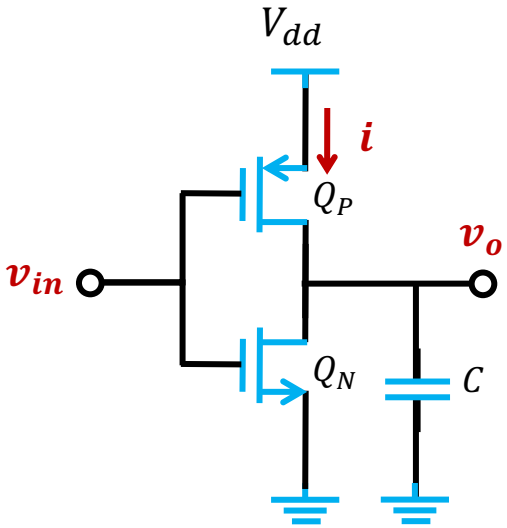


- @ $v_{in} = \frac{V_{dd}}{2}$ ➡ **Saturation region**

$$I_{peak} = \frac{1}{2}(\mu_n C_{ox})\left(\frac{W}{L}\right)_n \left(\frac{V_{dd}}{2} - V_{th,n}\right)^2$$

Another source of dynamic power

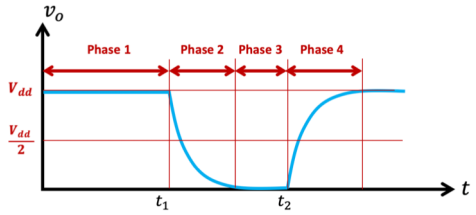
Summary: Power Consumption



- **STATIC POWER**

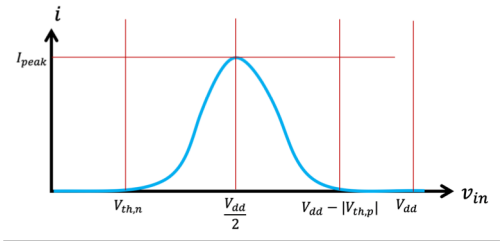
  Negligible low ➡ **Key advantage of CMOS circuits**

- **DYNAMIC POWER**



Source 1 – gate switching

$$P_{dyn} = fCV_{dd}^2$$

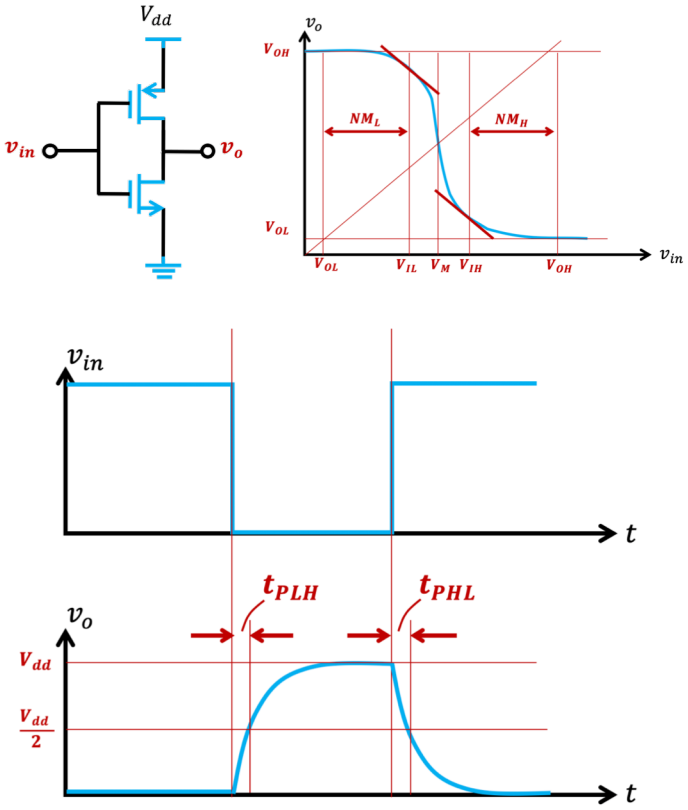


Source 2 – current through both transistors

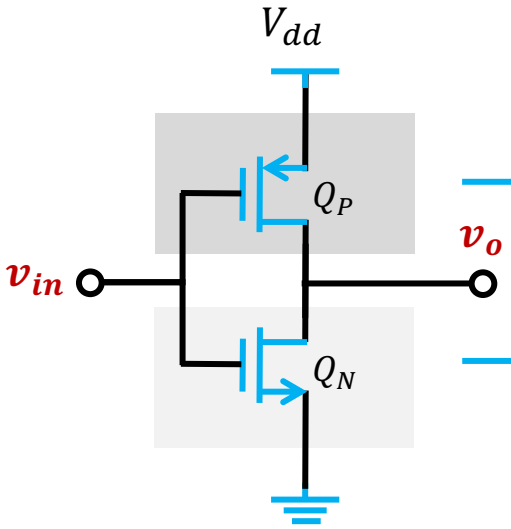
$$I_{peak} = \frac{1}{2}k_n\left(\frac{V_{dd}}{2} - V_{th,n}\right)^2$$

Outline

- CMOS Inverters
  - Voltage Transfer Characteristic (VTC)
  - Noise margin
  - Propagation delay
  - Power consumption
- **Logic-Gate Circuits**



CMOS Logic-Gate Circuits

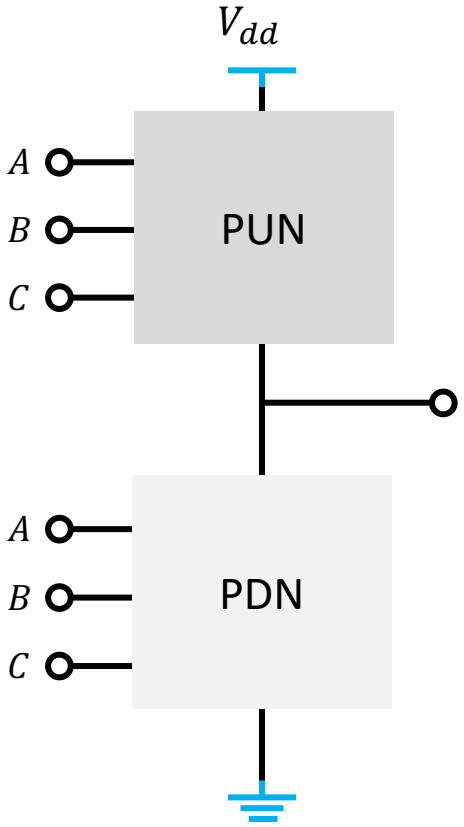


- **Pull-up network (PUN)**

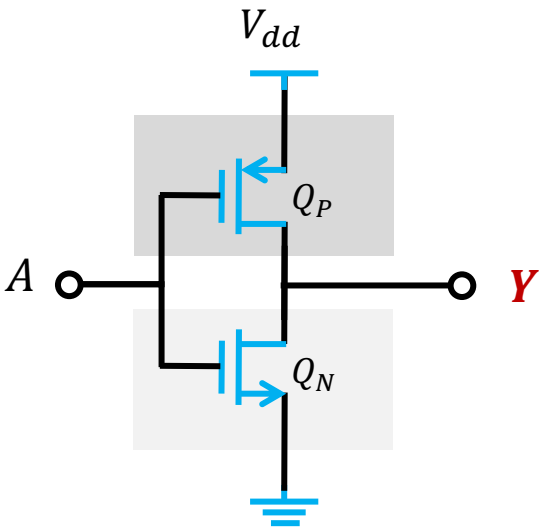
Constructed of PMOS

Constructed of NMOS

- **Pull-down network (PDN)**

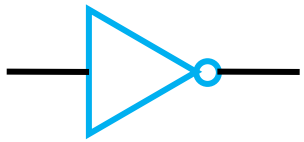


An Example of CMOS NOT Logic



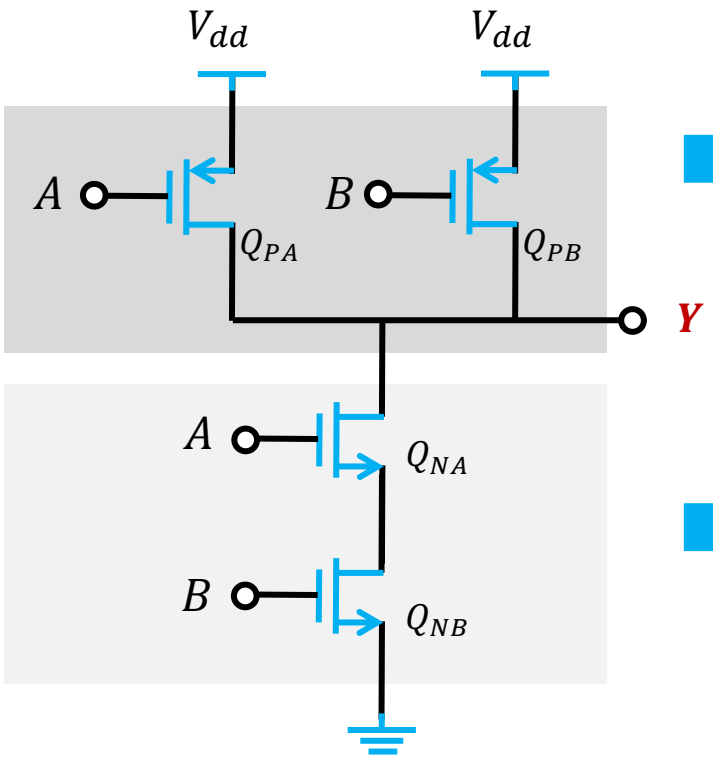
A	Y
V_{dd}	GND
GND	V_{dd}

$$Y = \overline{A}$$



Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



- **Pull-up network (PUN)**

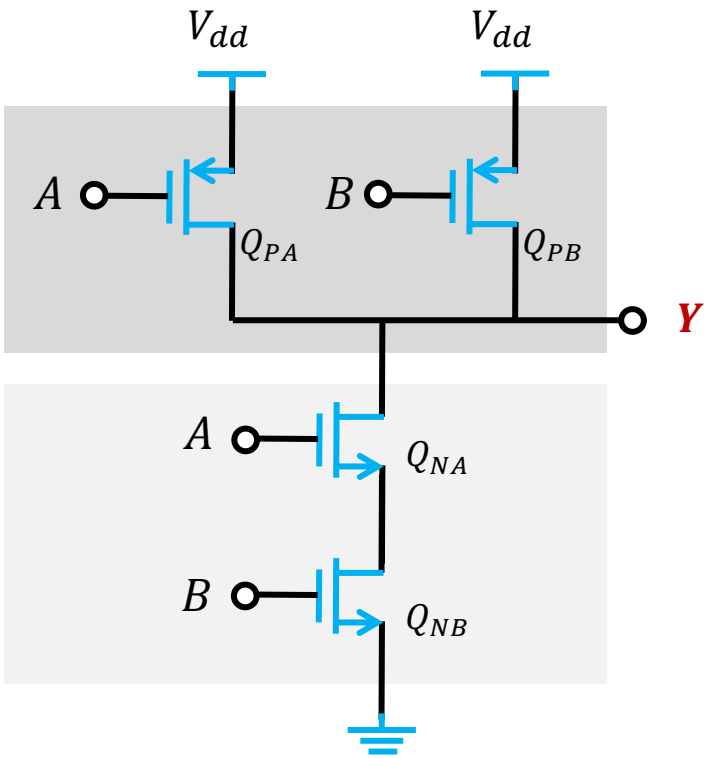
  Constructed of all PMOS

- **Pull-down network (PDN)**

  Constructed of all NMOS

Example 1: NAND gate circuit

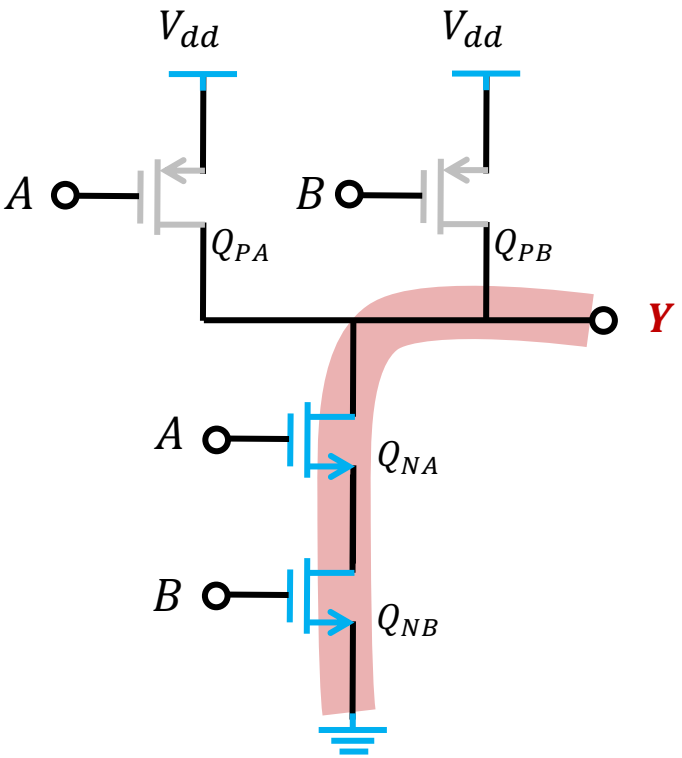
QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

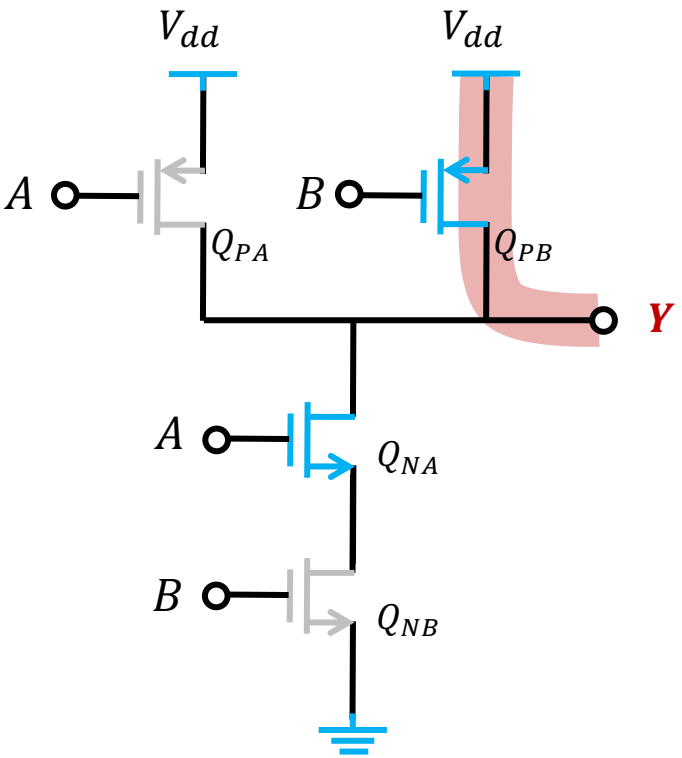
- @ $A = V_{dd}, B = V_{dd}$

  Q_{PA} is off Q_{PB} is off

  Q_{NA} is on Q_{NB} is on

Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	V_{dd}
GND	V_{dd}	
GND	GND	

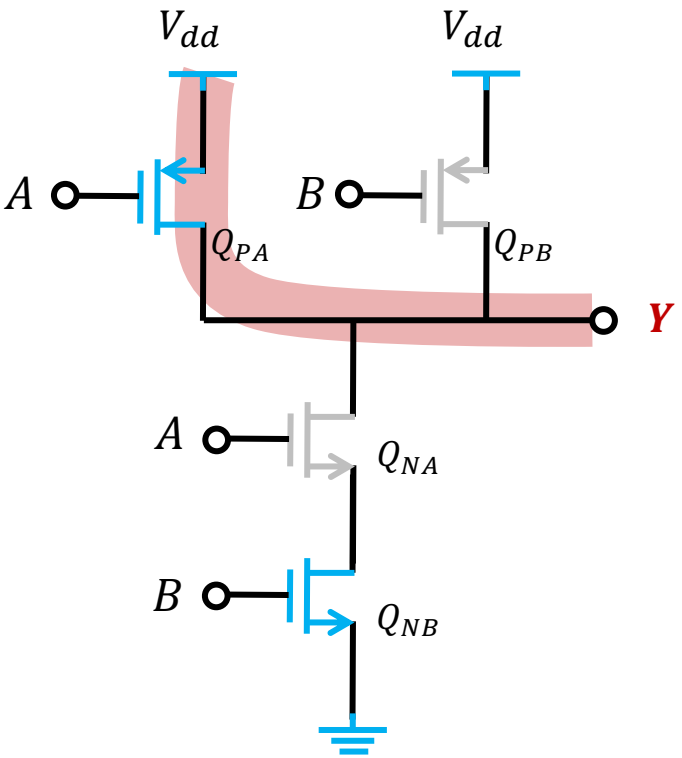
- @ $A = GND, B = V_{dd}$

  Q_{PA} is off Q_{PB} is on

  Q_{NA} is on Q_{NB} is off

Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	V_{dd}
GND	V_{dd}	V_{dd}
GND	GND	

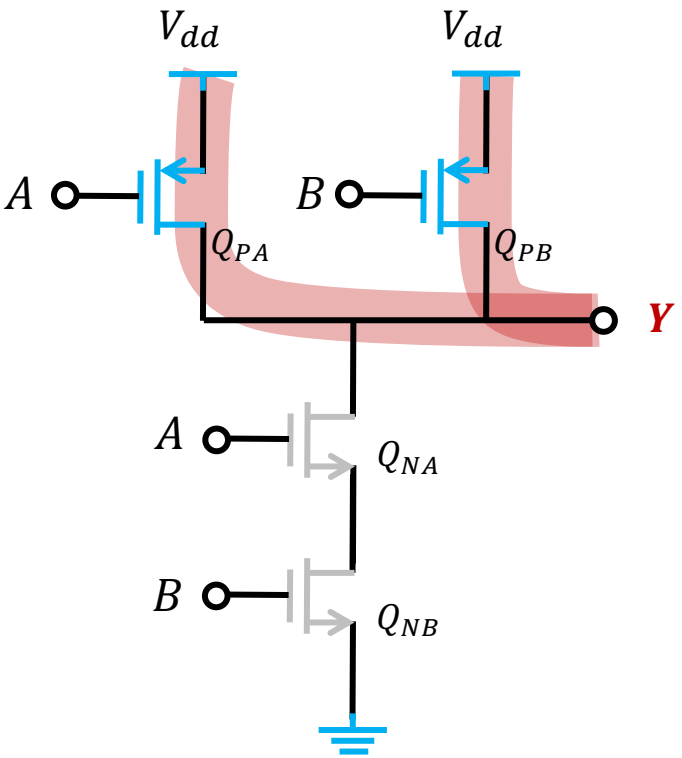
- @ $A = V_{dd}, B = GND$

  Q_{PA} is on Q_{PB} is off

  Q_{NA} is off Q_{NB} is on

Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	V_{dd}
GND	V_{dd}	V_{dd}
GND	GND	V_{dd}

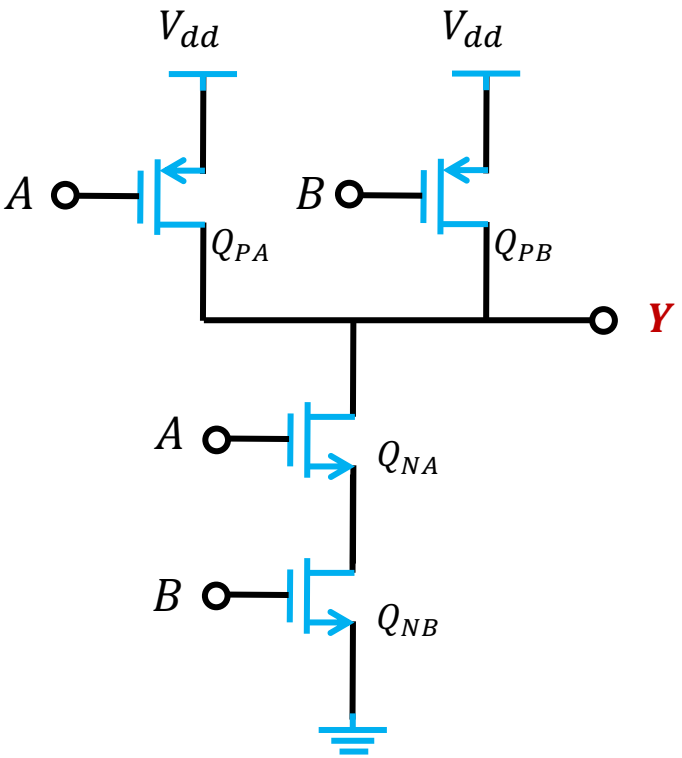
- @ $A = V_{dd}, B = V_{dd}$

  Q_{PA} is on Q_{PB} is off

  Q_{NA} is off Q_{NB} is on

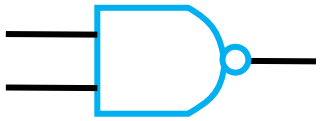
Example 1: NAND gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND

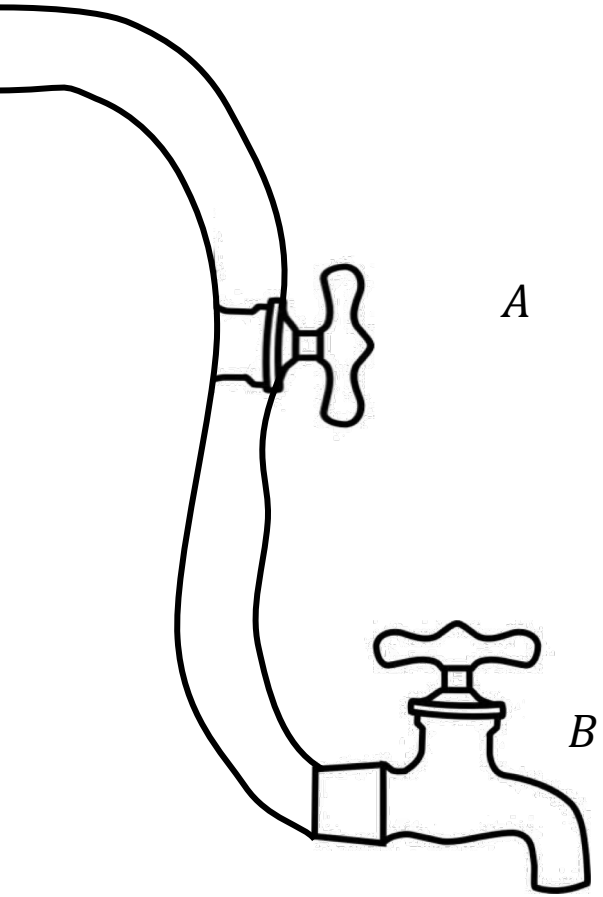


A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	V_{dd}
GND	V_{dd}	V_{dd}
GND	GND	V_{dd}

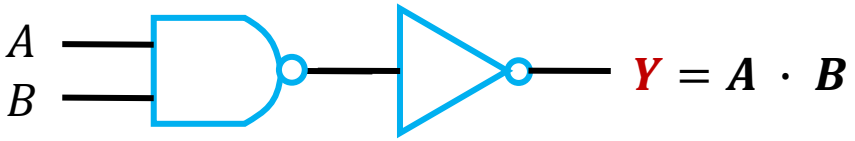
$$Y = \overline{A \cdot B}$$



An Example of AND Logic

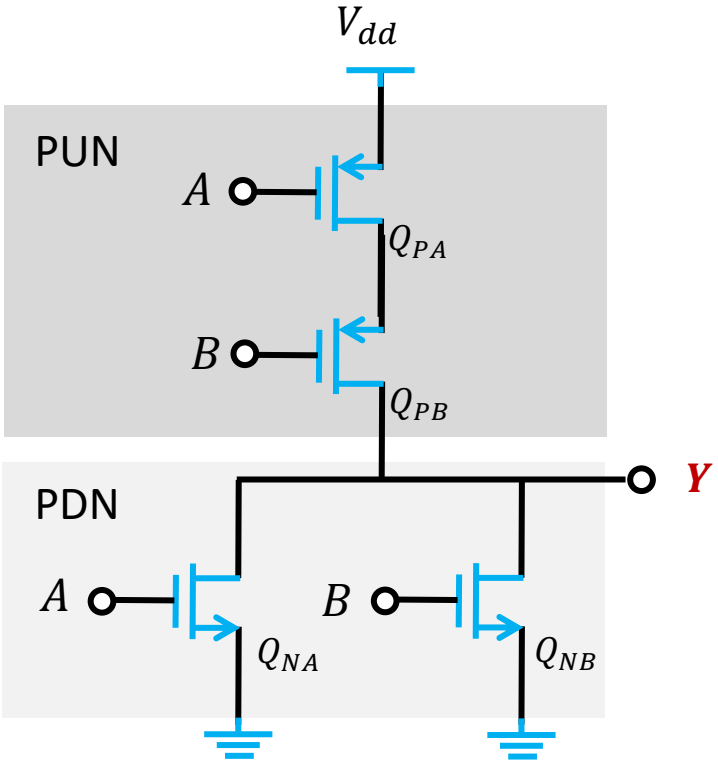


A	B	Y
On	On	**Water out**
On	Off	**No water**
Off	On	**No water**
Off	Off	**No water**



Example 2: NOR gate circuit

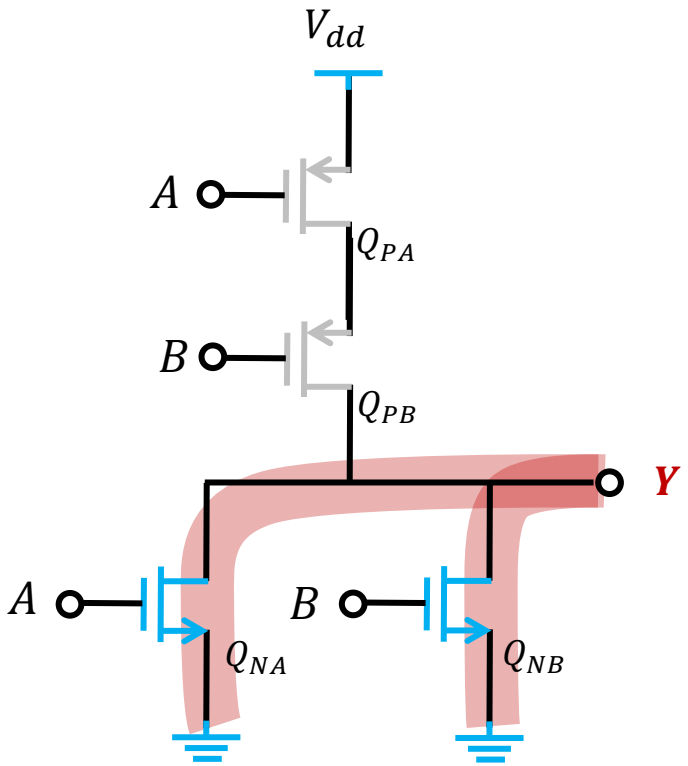
QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

Example 2: NOR gate circuit

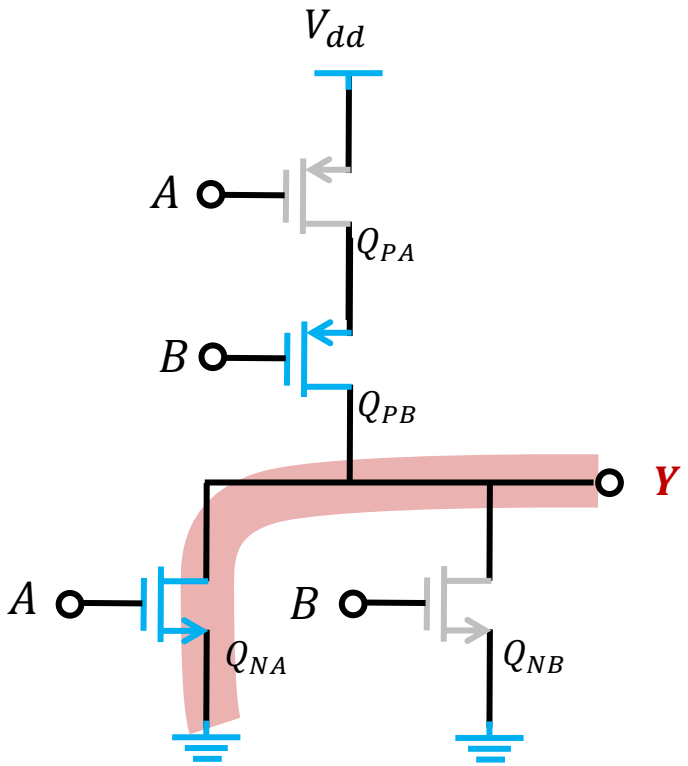
QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

Example 2: NOR gate circuit

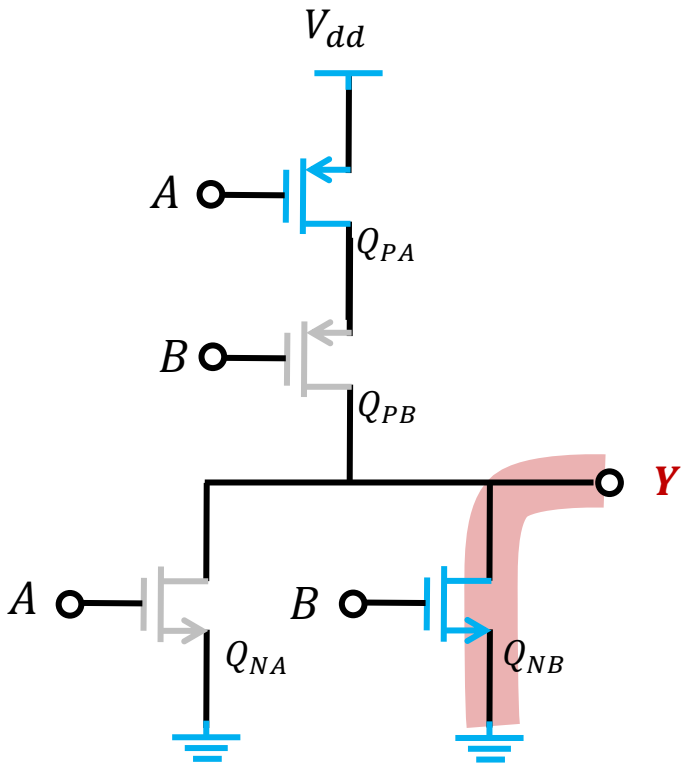
QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	
GND	GND	

Example 2: NOR gate circuit

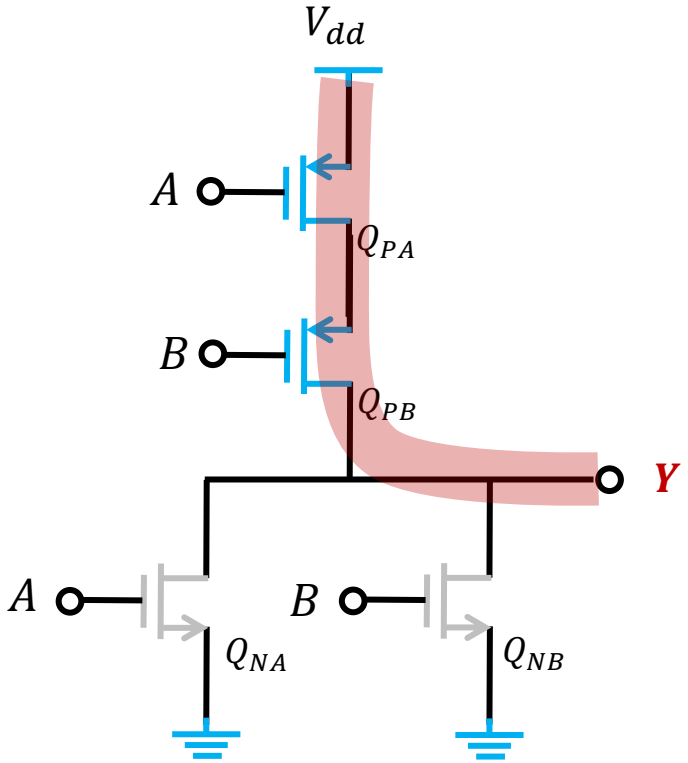
QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	

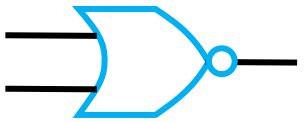
Example 2: NOR gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND

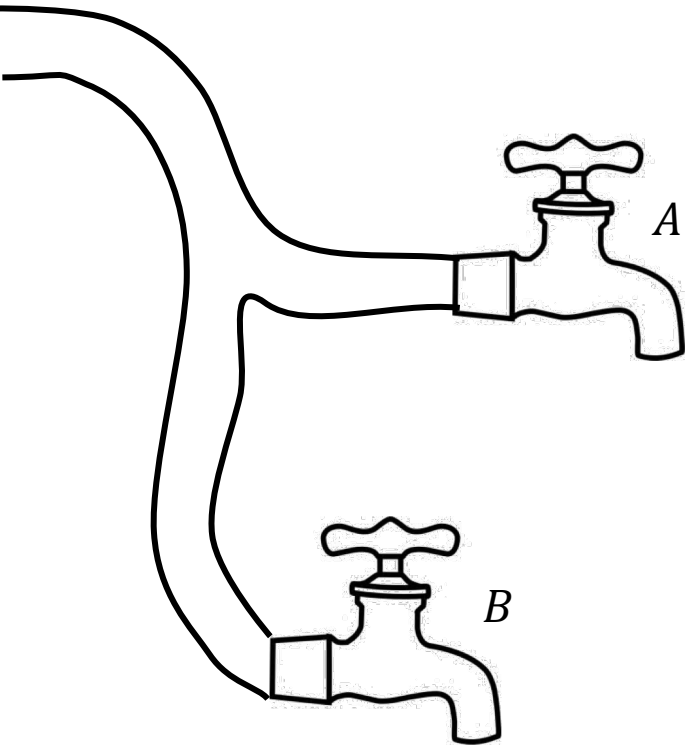


A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	V_{dd}

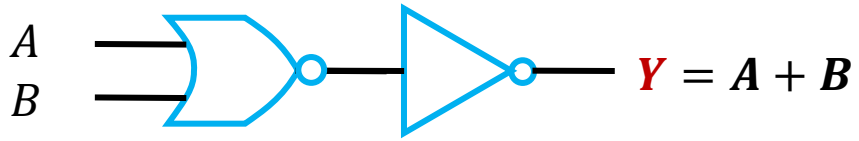
$$Y = \overline{A + B}$$



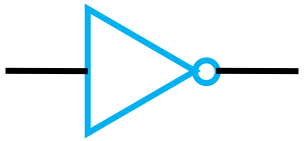
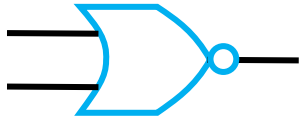
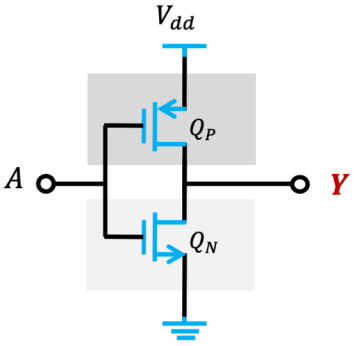
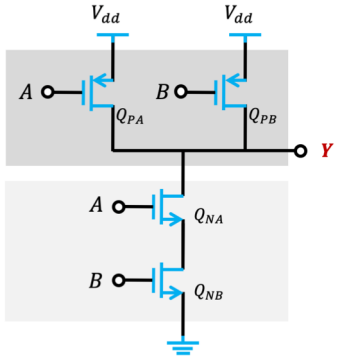
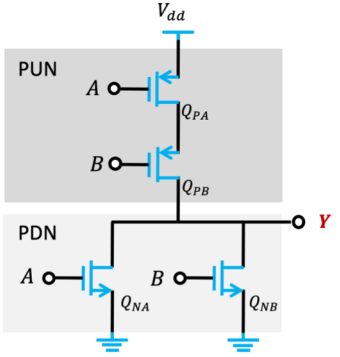
An Example of OR Logic



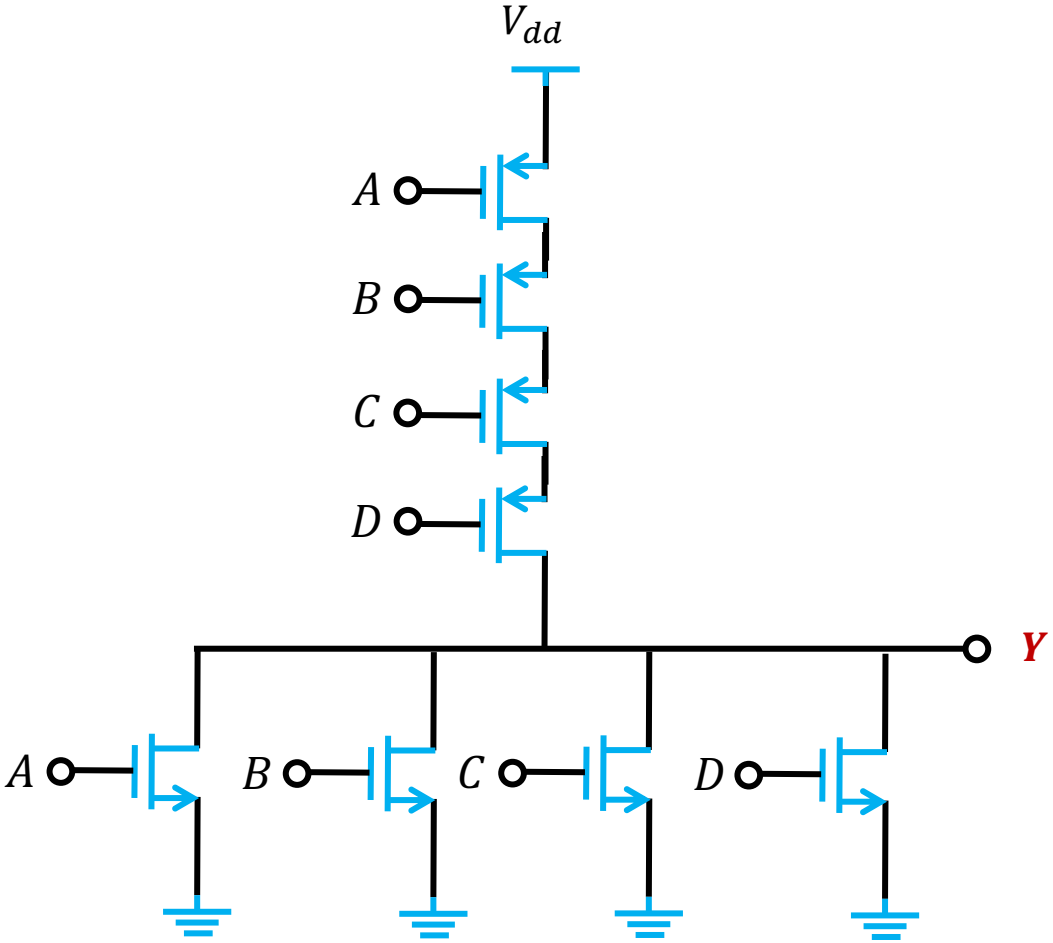
A	B	Y
On	On	**Water out**
On	Off	**Water out**
Off	On	**Water out**
Off	Off	**No water**



Summary: CMOS Logic-Gate Circuits

	NOT Logic Gate	NAND Logic Gate	NOR Logic Gate
Symbol			
Logic	$Y = \overline{A}$	$Y = \overline{A \cdot B}$	$Y = \overline{A + B}$
CMOS circuits			

Fan-In & Fan-Out

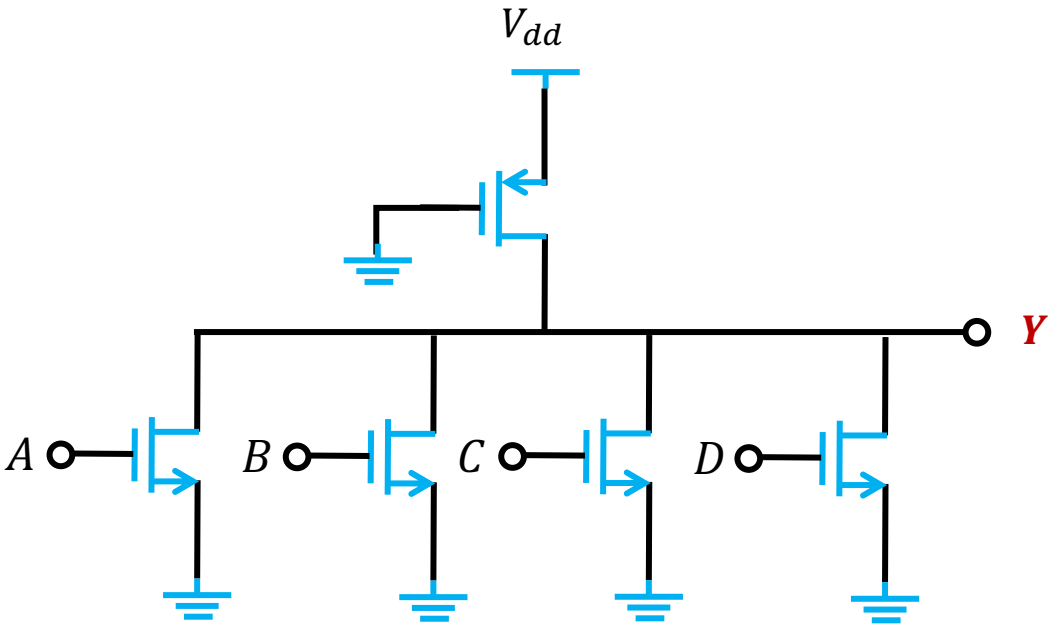


A 4-input NOR Gate

$$Y = \overline{A + B + C + D}$$

- **2** transistors required for **1** additional input
- An increasing of **silicon area**
- An increasing of the **capacitance**

Pseudo-NMOS Circuits



A 4-input NOR Gate

$$Y = \overline{A + B + C + D}$$

PROS

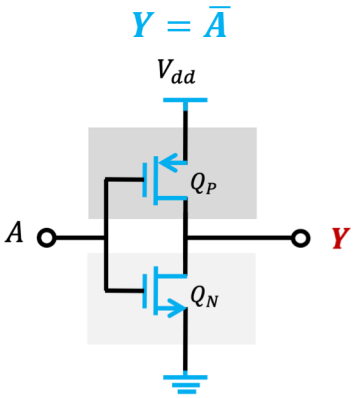
- 1 transistor for 1 additional input

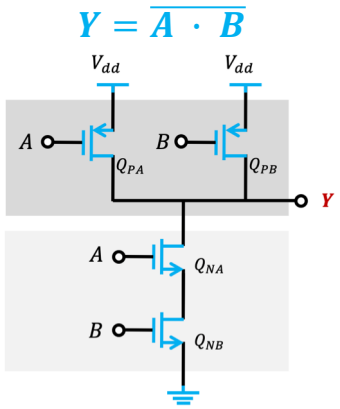
CONS

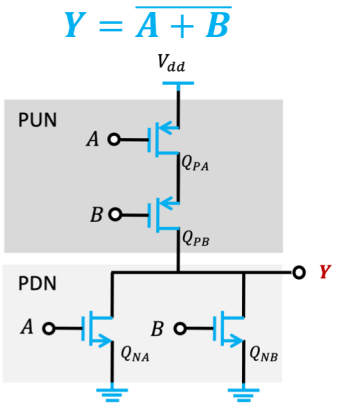
- Low logic swing
- Low noise margin
- High static power consumption

Outline

- CMOS Inverters
  - Voltage Transfer Characteristic (VTC)
  - Noise margin
  - Propagation delay
  - Power consumption
- Logic-Gate Circuits
- **Digital Switches & Dynamic Logic Circuits**



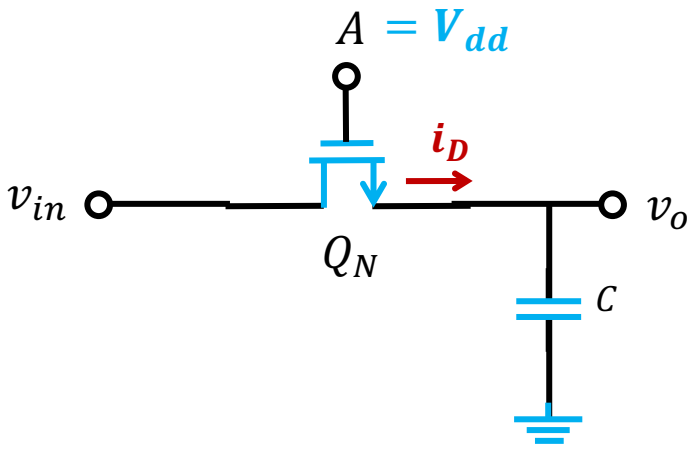


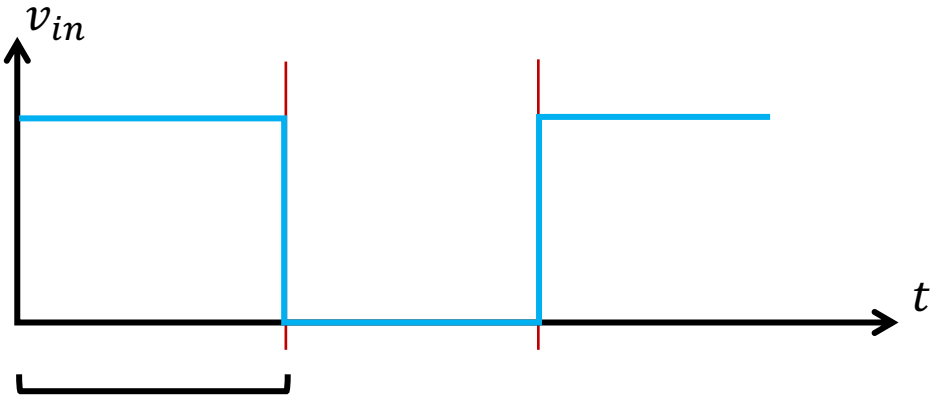


Outline

- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches & Dynamic Logic Circuits
  - **Single NMOS switch**

Single NMOS Switch



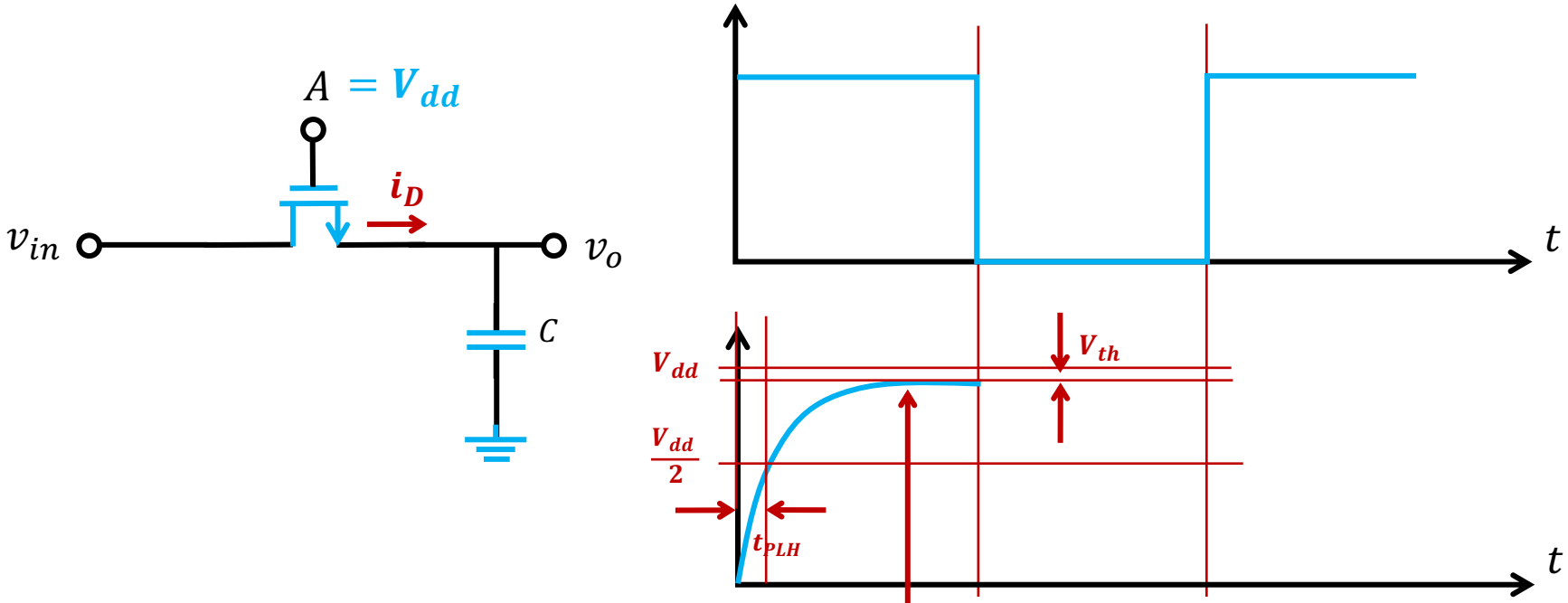


For Q_N, $v_{GS,N} - v_{DS,N} = 0 < V_{th,N}$

Assume $v_{GS,N} > V_{th,N}$

$$i_{DN} = \frac{1}{2} k_n \left(V_{dd} - v_o - V_{th,N}\right)^2$$

Single NMOS Switch



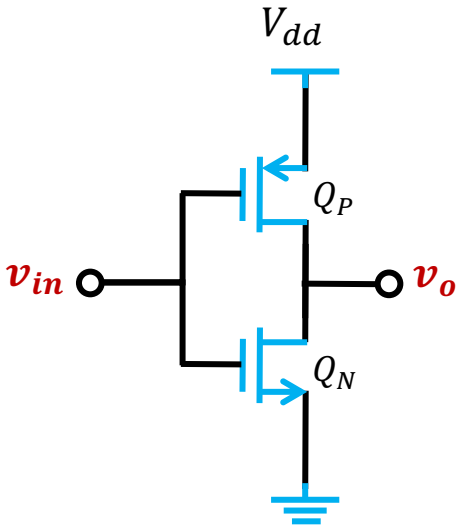
For Q_N, $v_{GS,N} - v_{DS,N} = 0 < V_{th,N}$

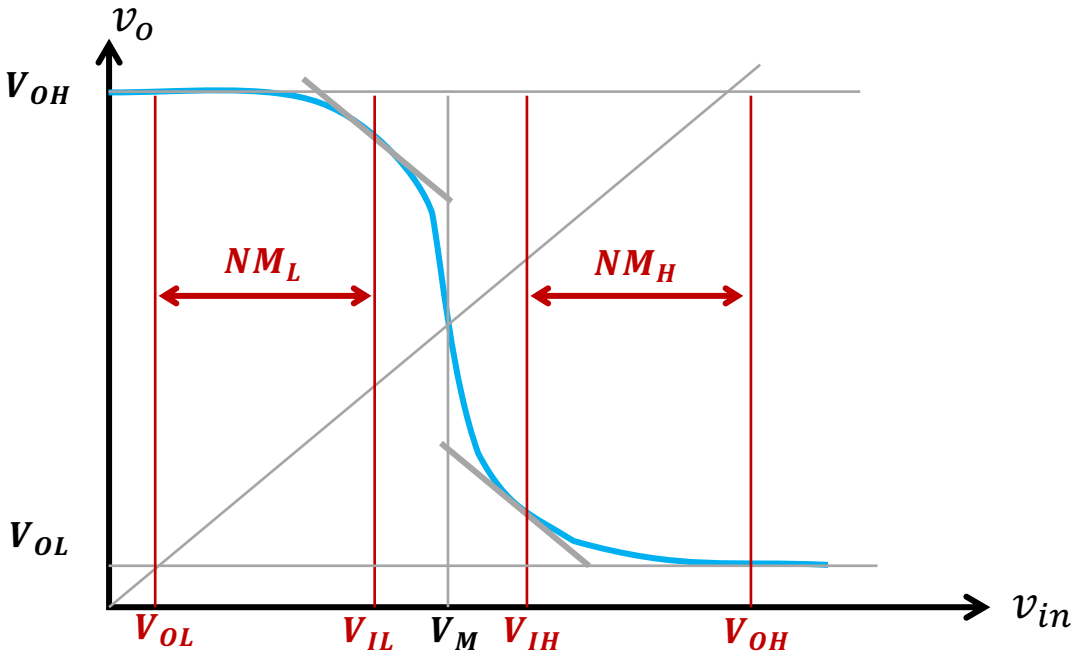
Assume $v_{GS,N} > V_{th,N}$

TRUE if $v_o < V_{dd} - V_{th,N}$

$$i_{DN} = \frac{1}{2} k_n \left(V_{dd} - v_o - V_{th,N}\right)^2$$

Recall: Noise Margin



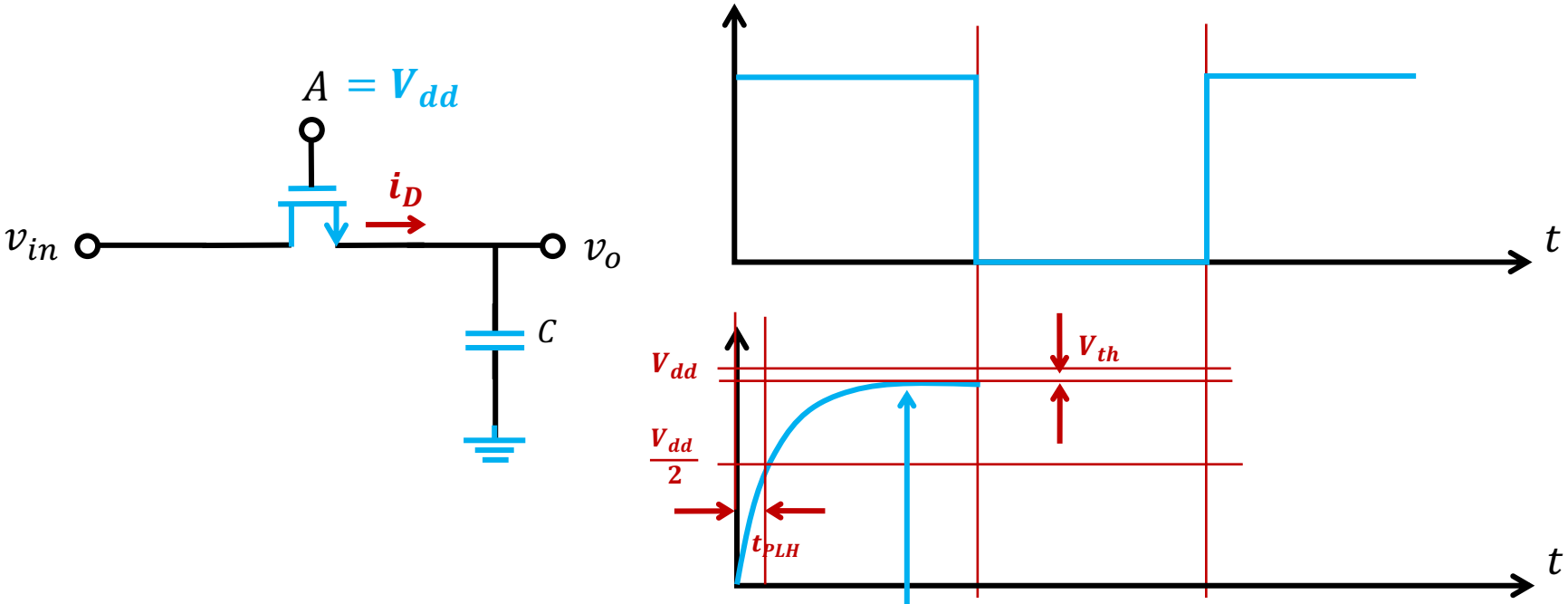


$$\begin{cases} V_{IH} = \dfrac{5V_{dd} - 2V_{th}}{8} \\ V_{IL} = \dfrac{3V_{dd} + 2V_{th}}{8} \end{cases}$$

$$NM_L = V_{IL} - \underbrace{V_{OL}}_{0} = \frac{3V_{dd} + 2V_{th}}{8}$$

$$NM_H = \underbrace{V_{OH}}_{V_{dd}} - V_{IH} = \frac{3V_{dd} + 2V_{th}}{8}$$

Single NMOS Switch



For Q_N, $v_{GS,N} - v_{DS,N} = 0 < V_{th}$

Assume $v_{GS,N} > V_{th}$

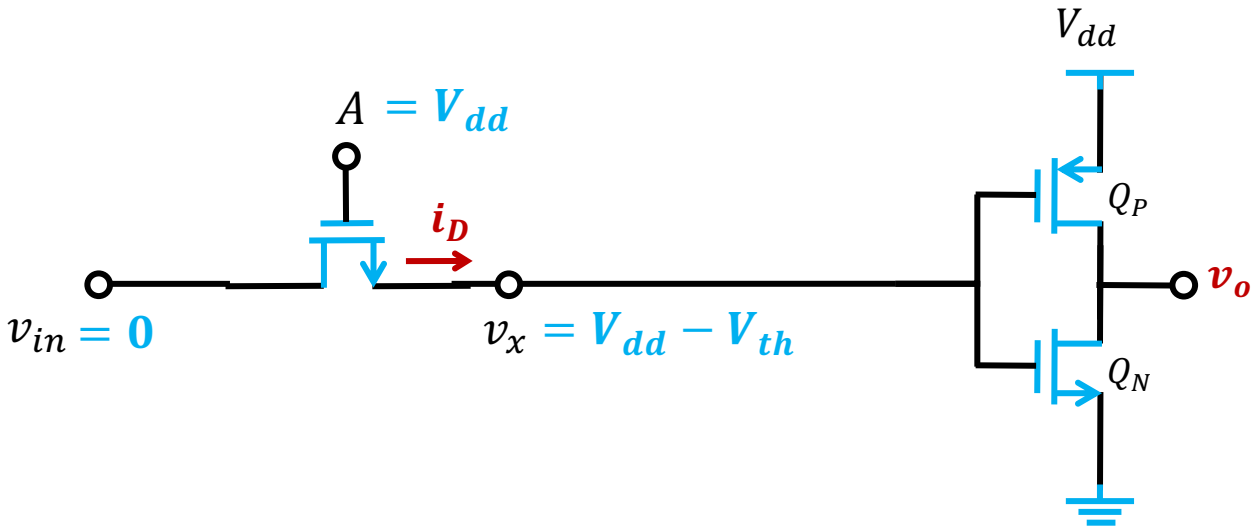
$$i_{DN} = \frac{1}{2} k_n (V_{dd} - v_o - V_{th})^2$$

TRUE if $v_o < V_{dd} - V_{th}$

V_{OH} is only $V_{dd} - V_{th}$ instead of V_{dd}

☹ Noise margin performance

Single NMOS Switch

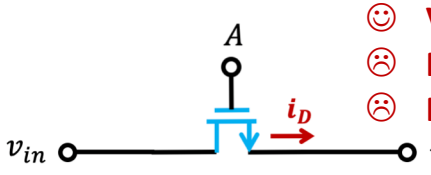


Q_P is ON since $|v_{GS,P}| = V_{th,P}$ ➡ Unexpected static power

☹ **Static power consumption performance**

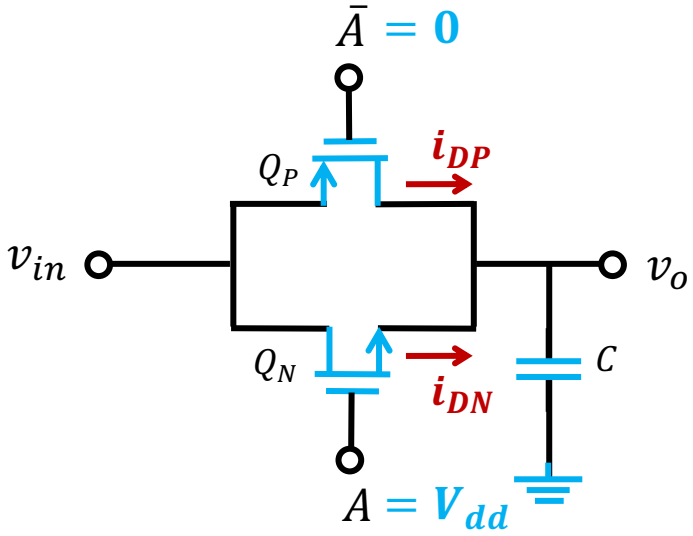
Outline

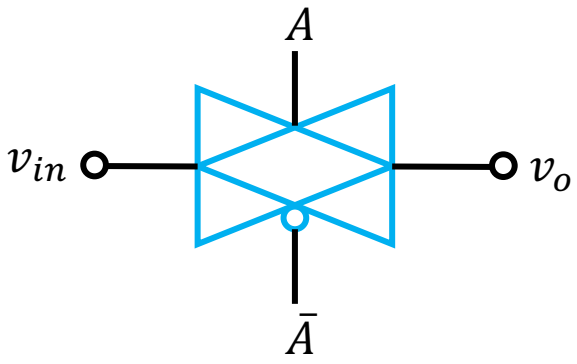
- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches & Dynamic Logic Circuits
  - Single NMOS switch
  - **Transmission Gate Switch**

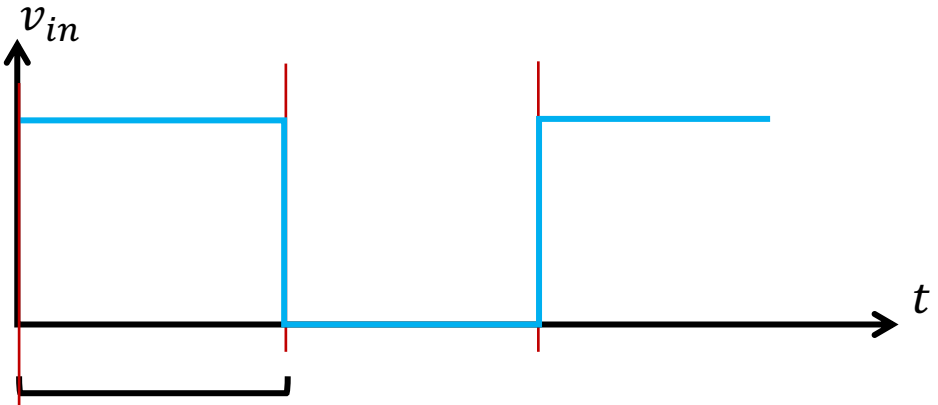


☺ **Very Simple**
☹ **Noise margin**
☹ **Power Consumption**

Transmission Gate Switch







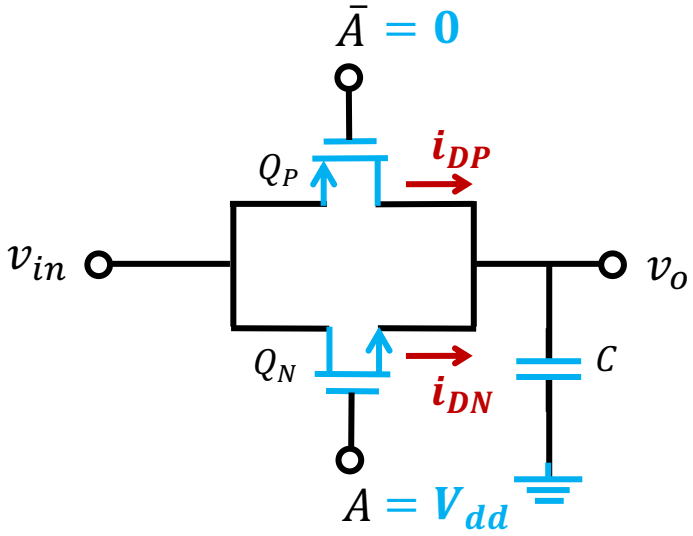
For Q_N, $v_{GS,N} - v_{DS,N} = 0 < V_{th,N}$

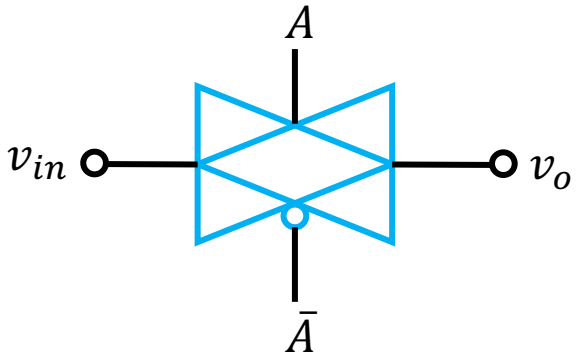
Assume $v_{GS,N} > V_{th,N}$

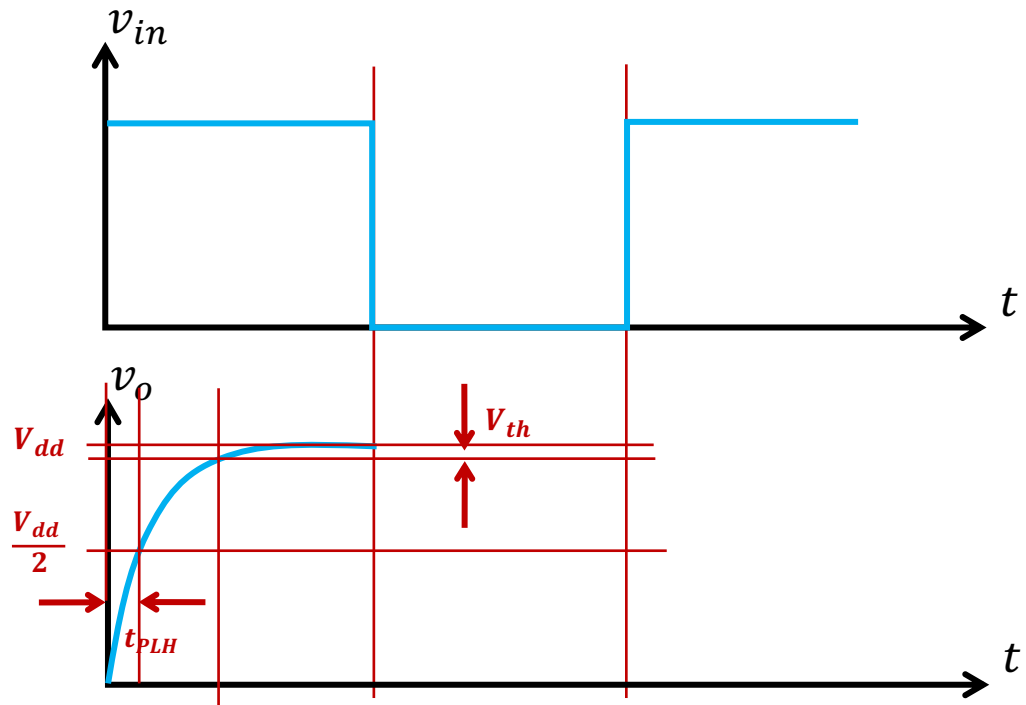
Q_N is biased in saturation region

$$i_{DN} = \frac{1}{2} k_n \left(V_{dd} - v_o - V_{th,N}\right)^2$$

Transmission Gate Switch







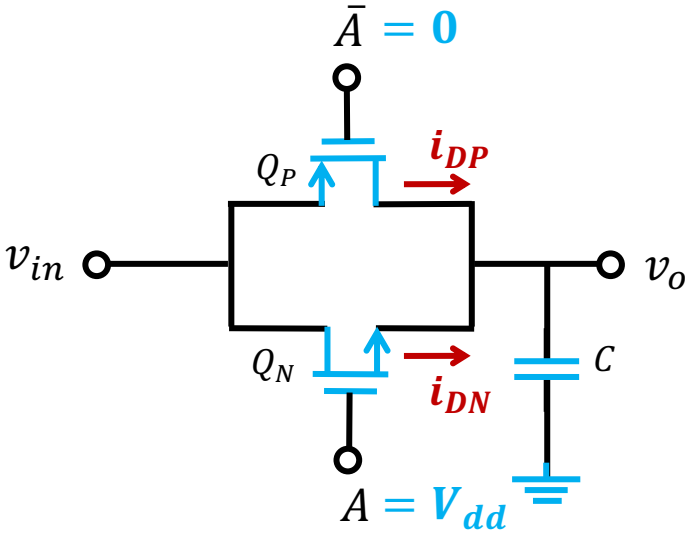
When $v_o = V_{dd} - V_{th,N}$

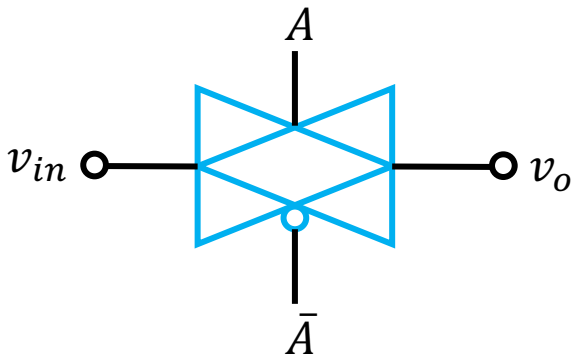
$i_{DN} = 0$

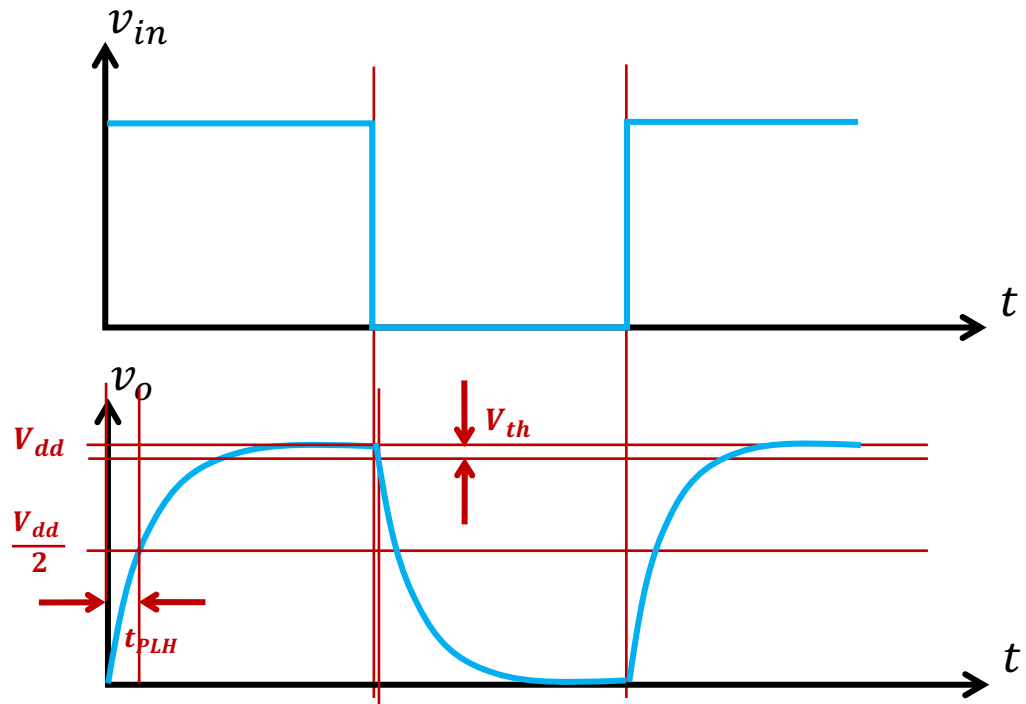
Q_P is ON

i_{DP} charges C to V_{dd}

Transmission Gate Switch



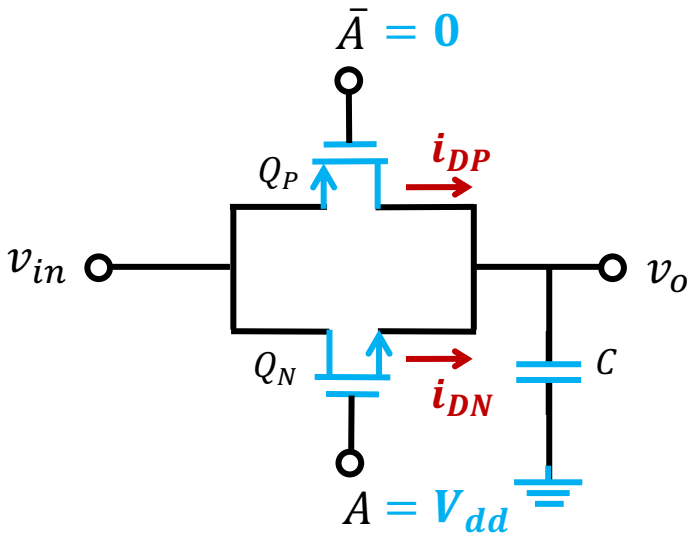




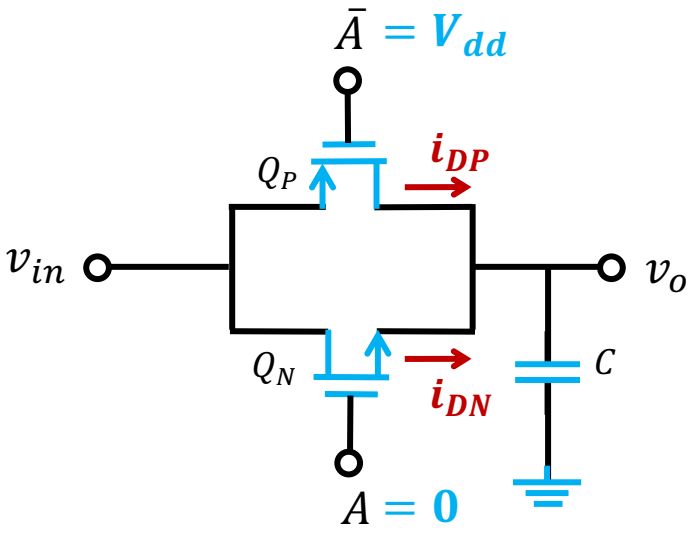
Q_P is ON

i_{DP} discharges C to 0

Transmission Gate Switch



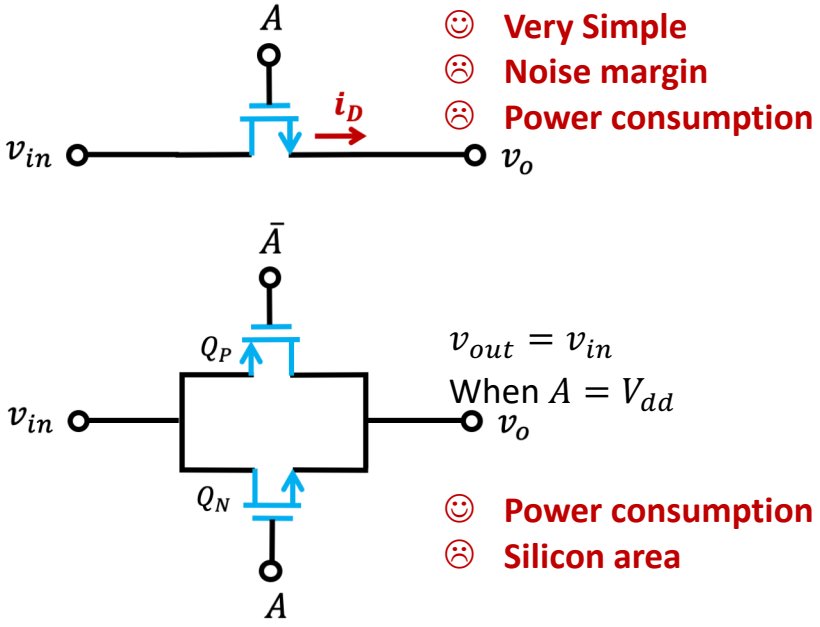
$v_{out} = v_{in}$



Both Q_N and Q_P are turned off

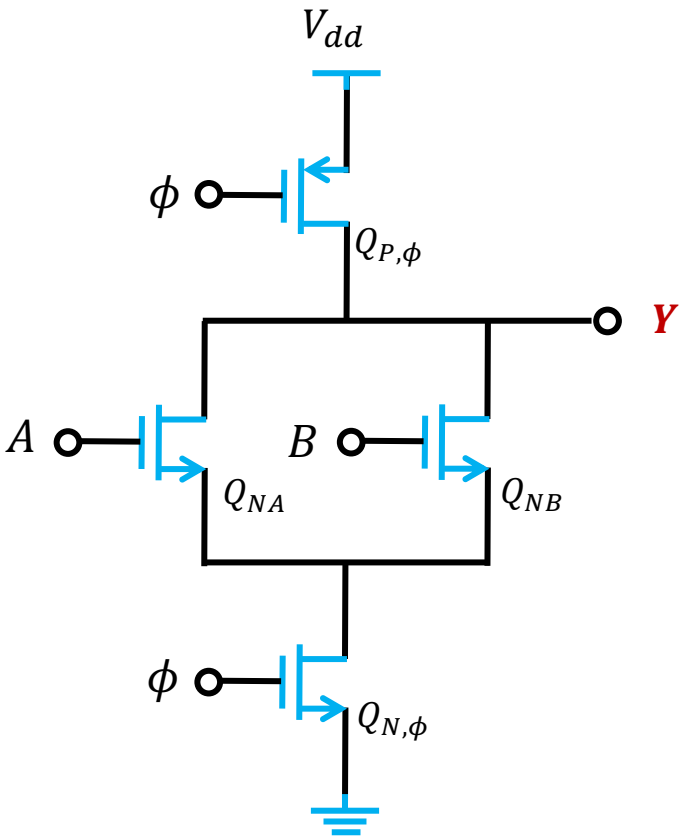
Outline

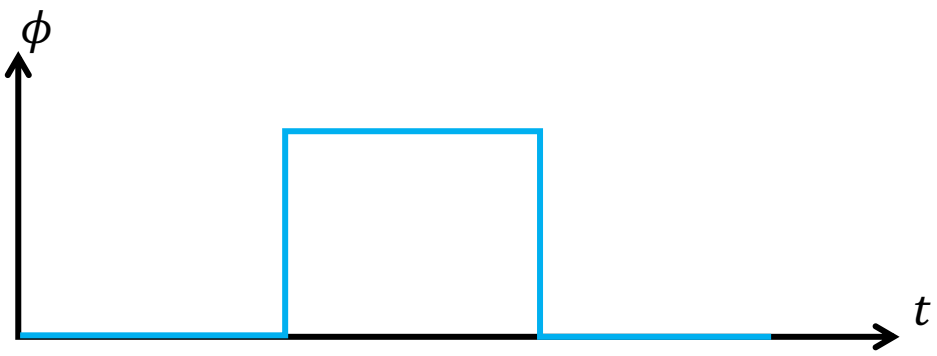
- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches &
  Dynamic Logic Circuits
  - Single NMOS switch
  - Transmission Gate Switch
  - **Dynamic logic circuits**



Example 3: Dynamic MOS Logic

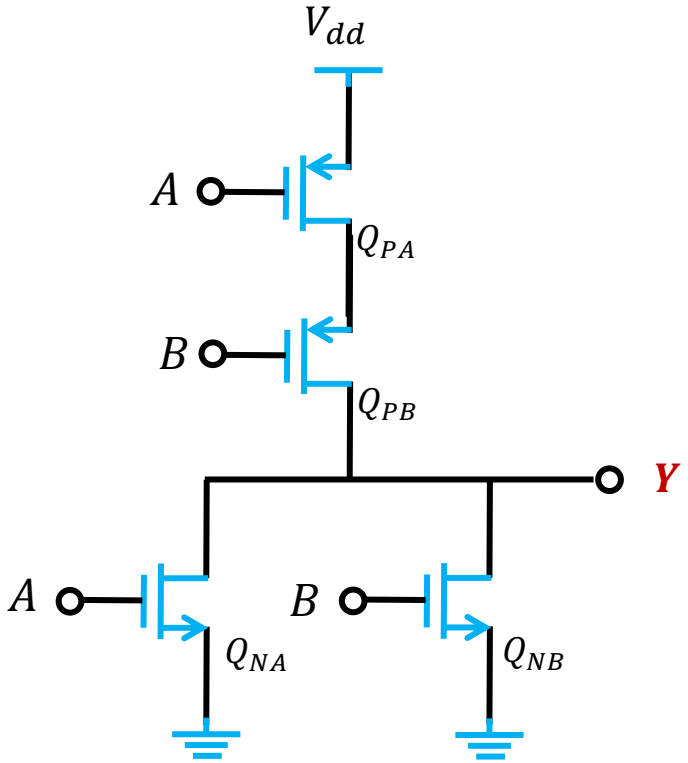
QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND





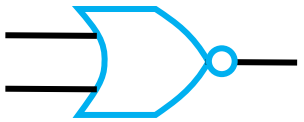
Recall: NOR gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



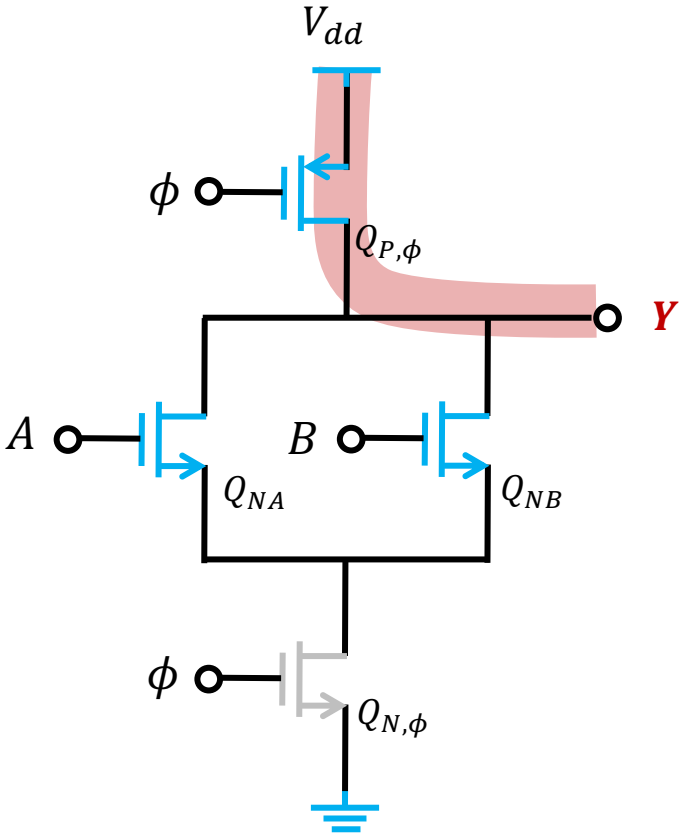
A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	V_{dd}

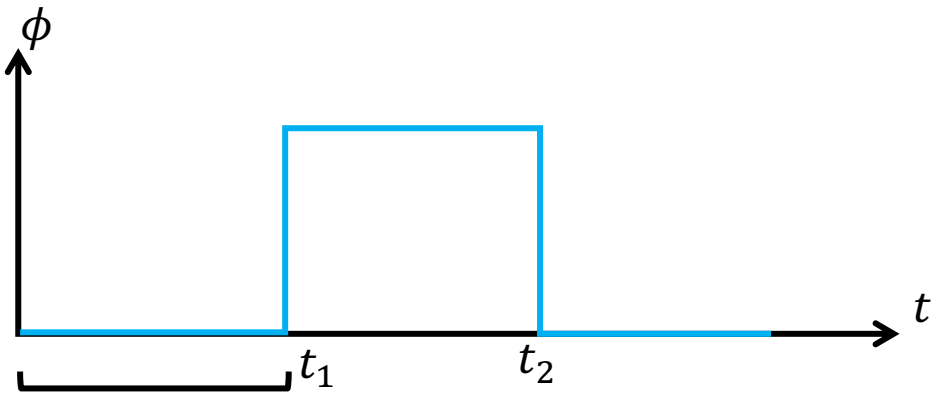
$$Y = \overline{A + B}$$



Example 3: Dynamic MOS Logic

QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND





$Q_{P,\phi}$ is ON since $|v_{GS,P}| = V_{dd} > V_{th,P}$

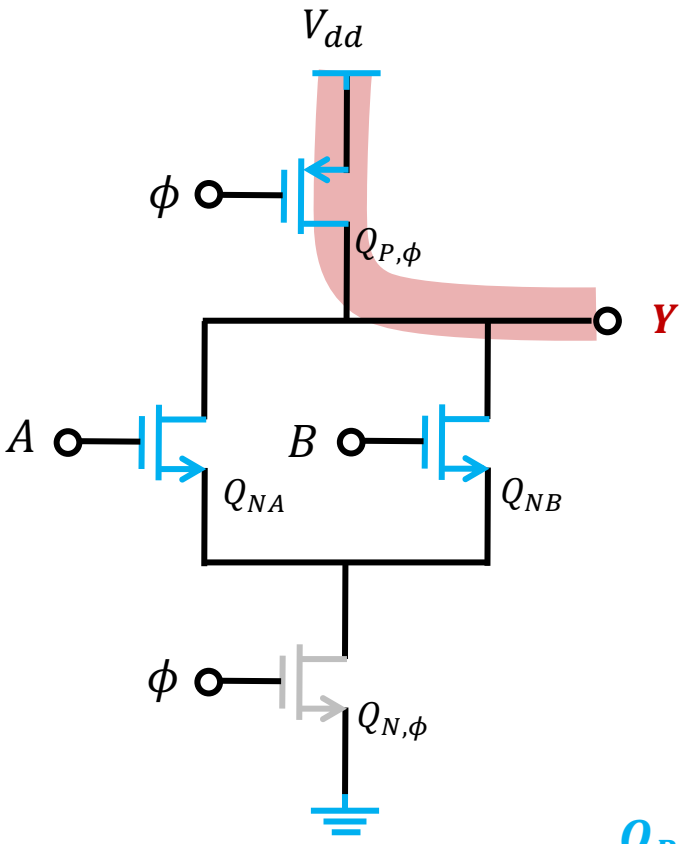
If $Y = 0$ @ $t = 0$

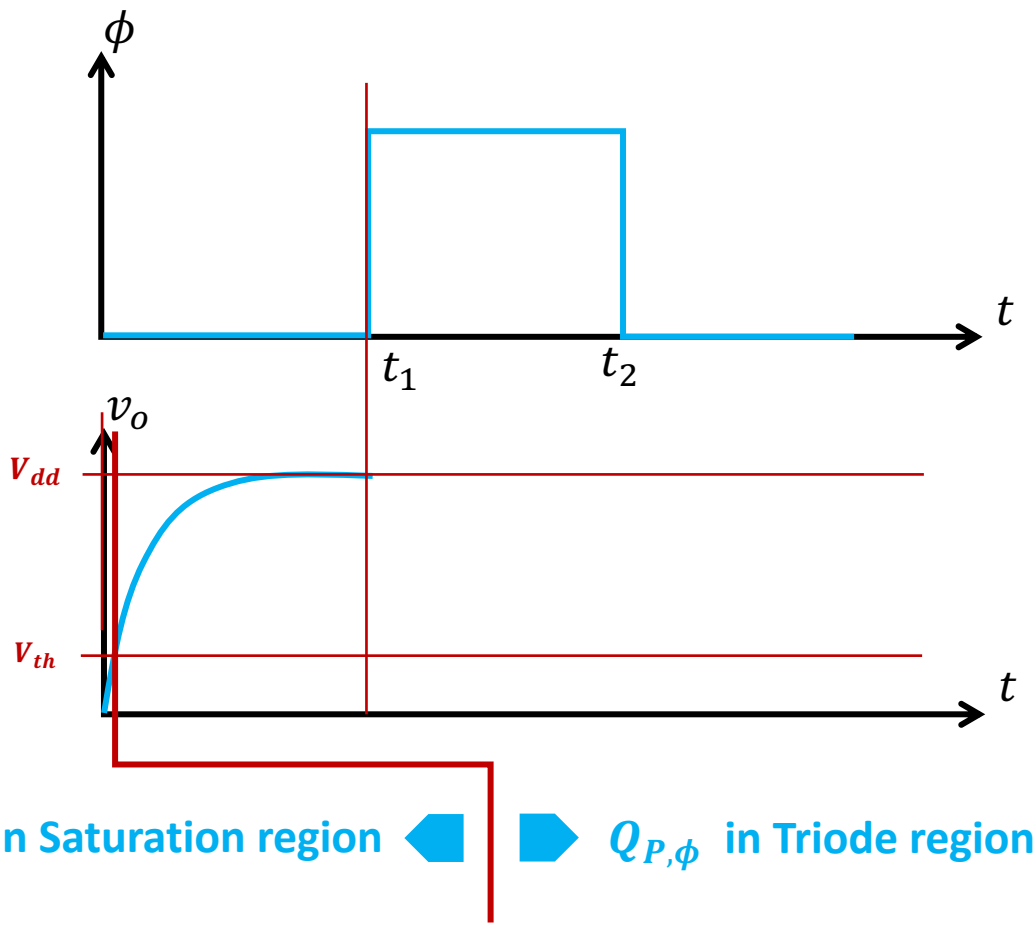
$|v_{DS,P}| > |v_{GS,P}| - V_{th}$ ➡ **Saturation**

$$i_D = \frac{1}{2} k_p \left(|v_{GS,P}| - V_{th,P}\right)^2$$

Example 3: Dynamic MOS Logic

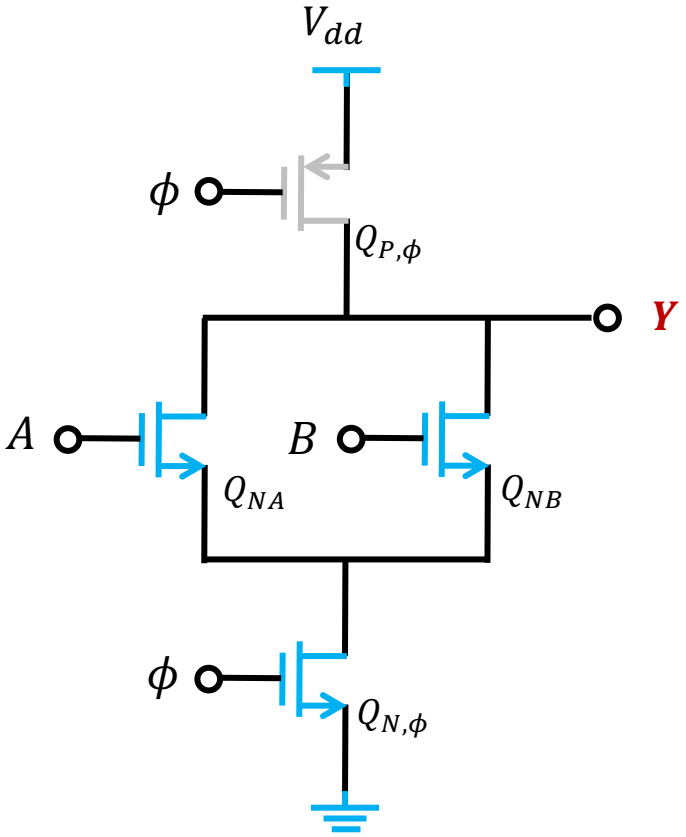
QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND

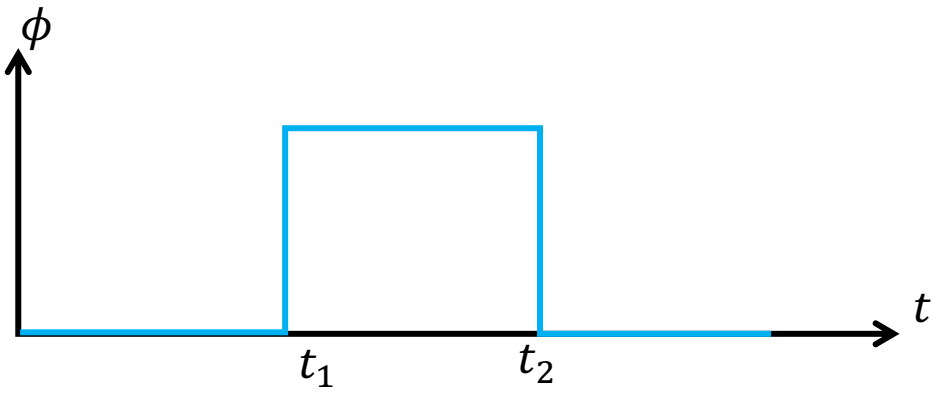




Example 3: Dynamic MOS Logic

QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND





$@\ t = t_1^-$ $\quad Y = V_{dd}$

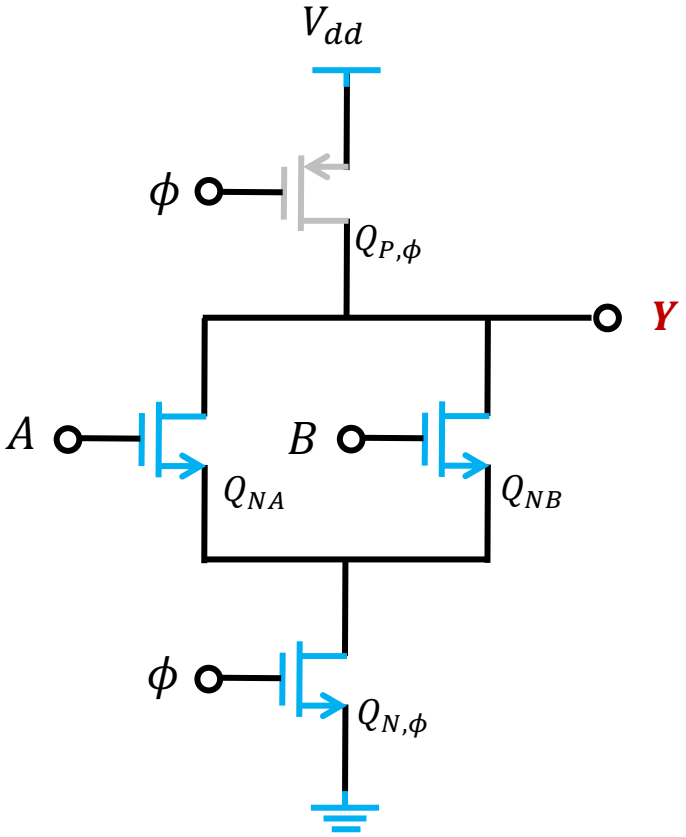
$@\ t = t_1^+$ $\quad Y = V_{dd}$

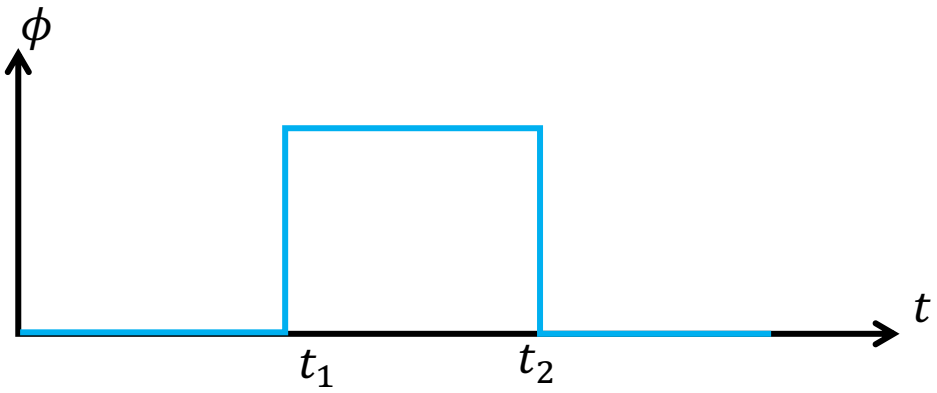
$Q_{P,\phi}$ is OFF

$Q_{N,\phi}$ is ON

Example 3: Dynamic MOS Logic

QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND

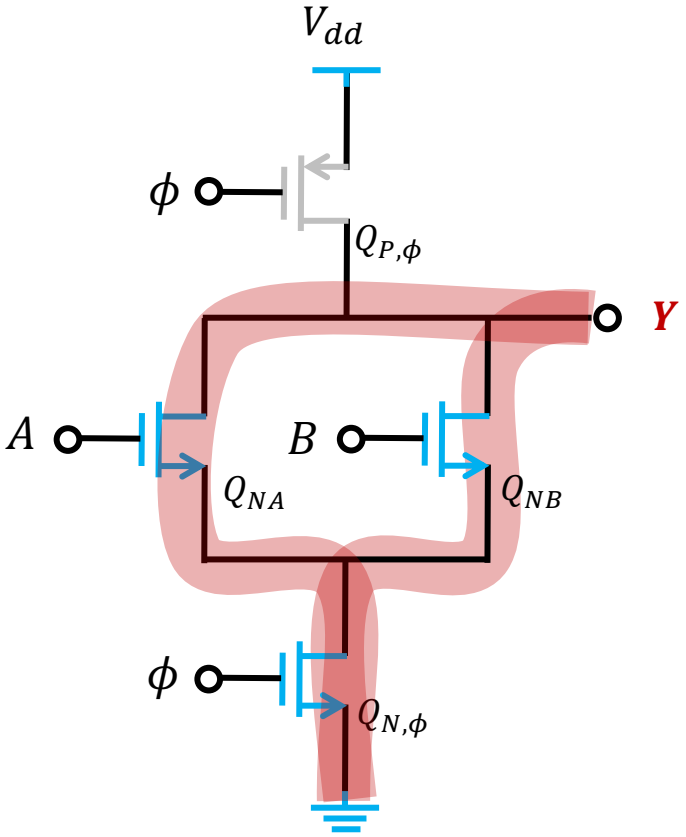


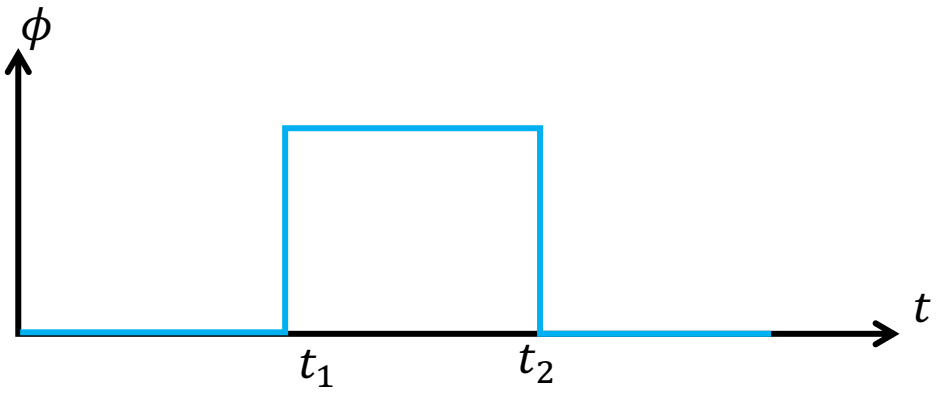


A	B	Y
V_{dd}	V_{dd}	
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

Example 3: Dynamic MOS Logic

QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND

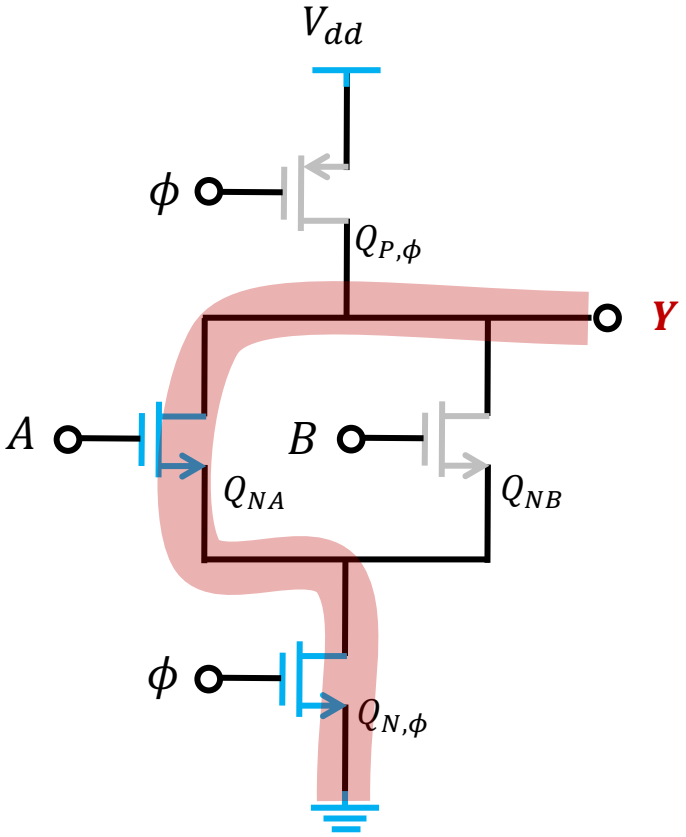


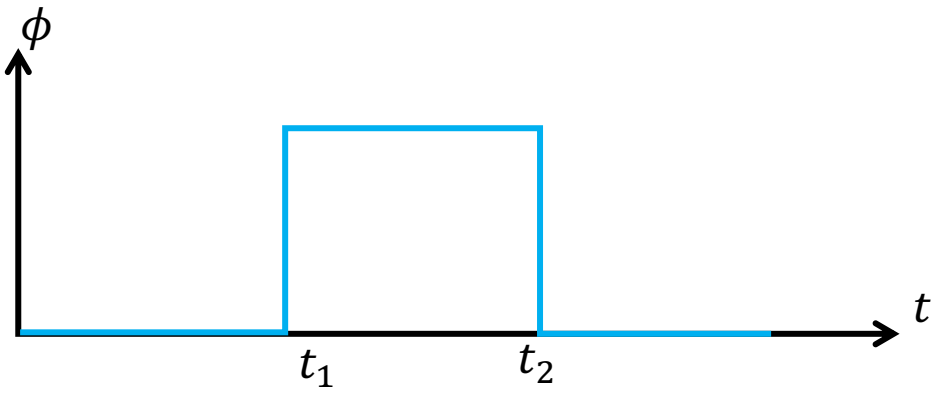


A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	
GND	V_{dd}	
GND	GND	

Example 3: Dynamic MOS Logic

QUESTION: Find out the output Y with different combination of the inputs. ϕ is a clock signal. The inputs switch between V_{dd} and GND





A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	
GND	GND	

Example 3: Dynamic MOS Logic

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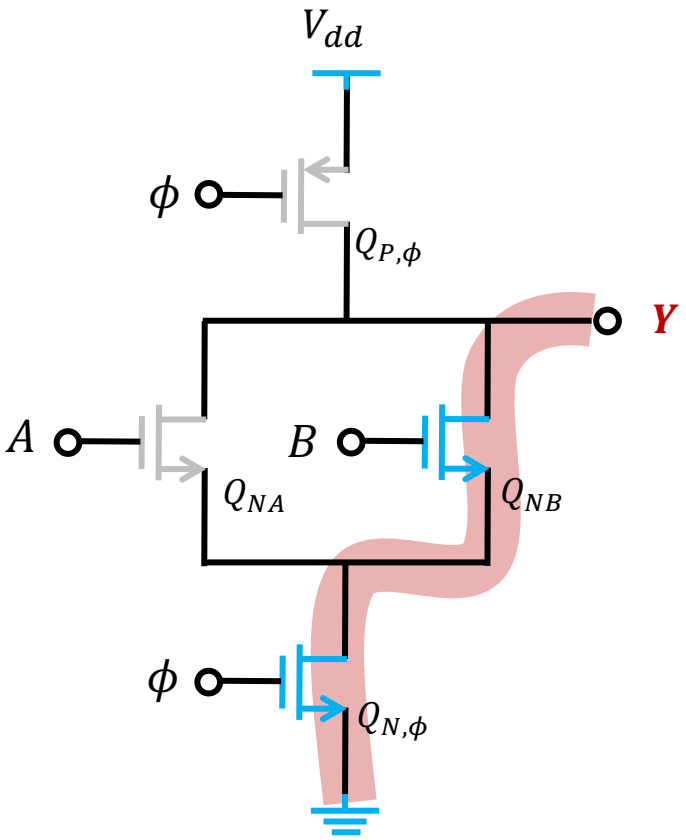

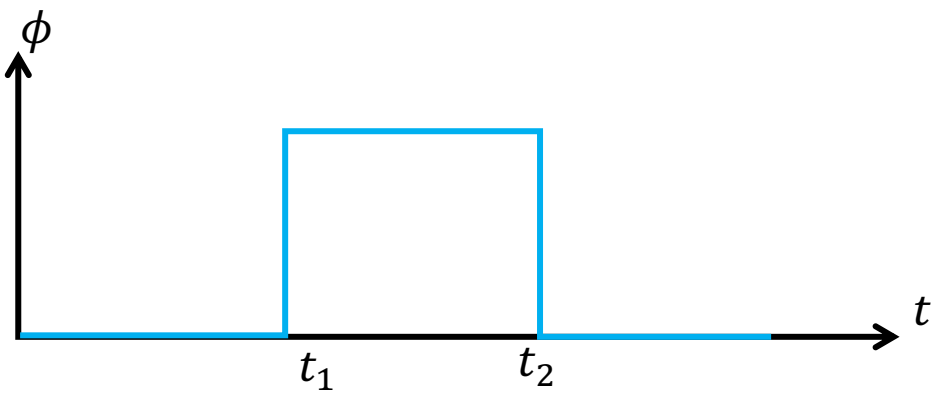

A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	

Example 3: Dynamic MOS Logic

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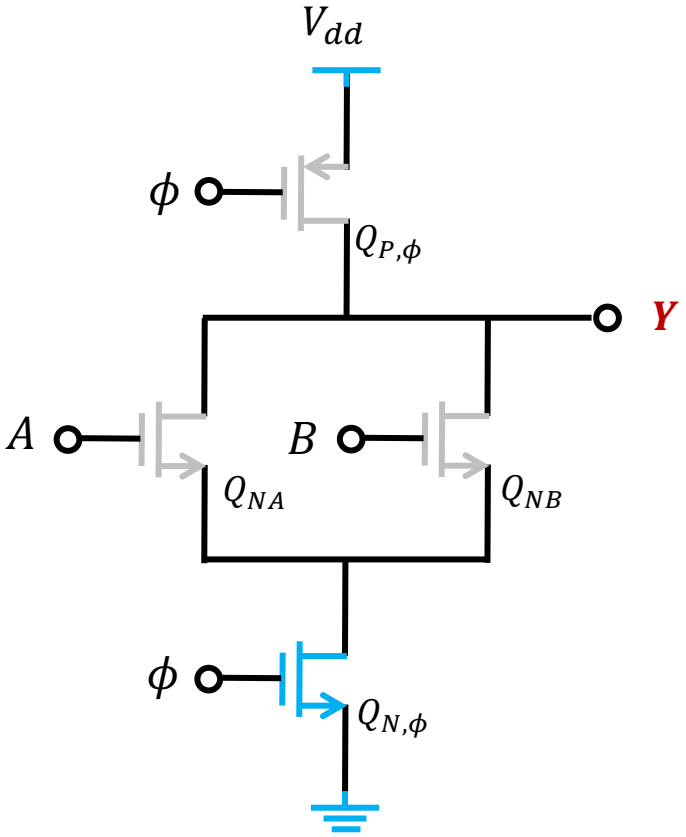
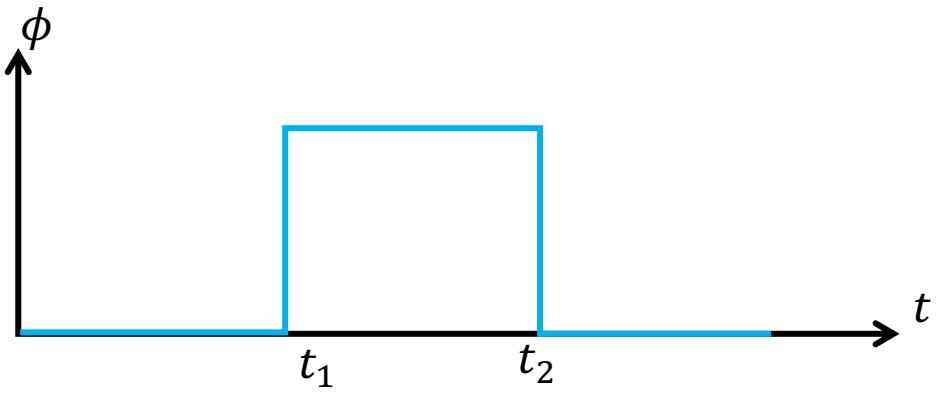
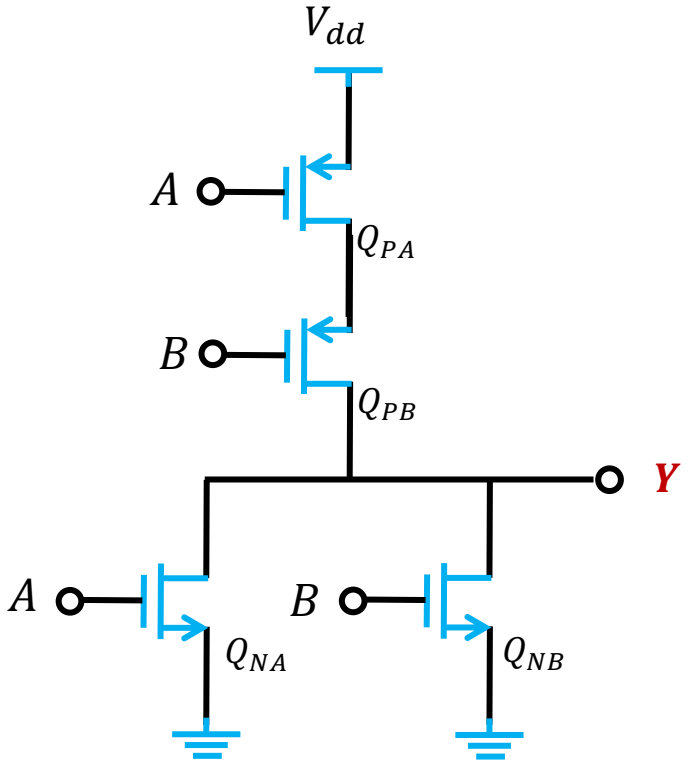




A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	V_{dd}

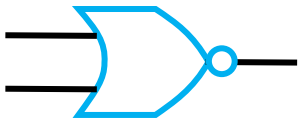
Recall: NOR gate circuit

QUESTION: Find out the output Y with different combination of the inputs. The inputs switch between V_{dd} and GND



A	B	Y
V_{dd}	V_{dd}	GND
V_{dd}	GND	GND
GND	V_{dd}	GND
GND	GND	V_{dd}

$$Y = \overline{A + B}$$



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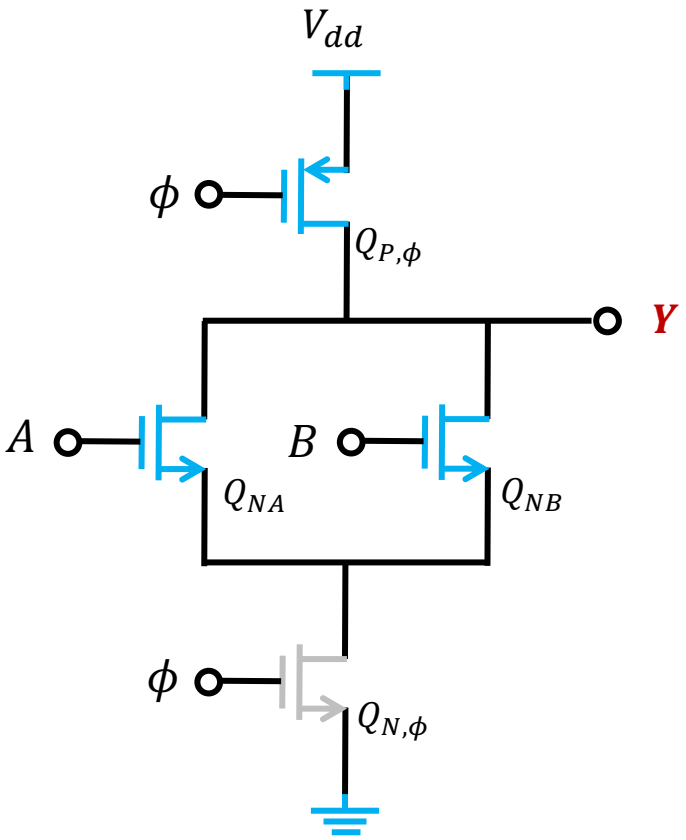
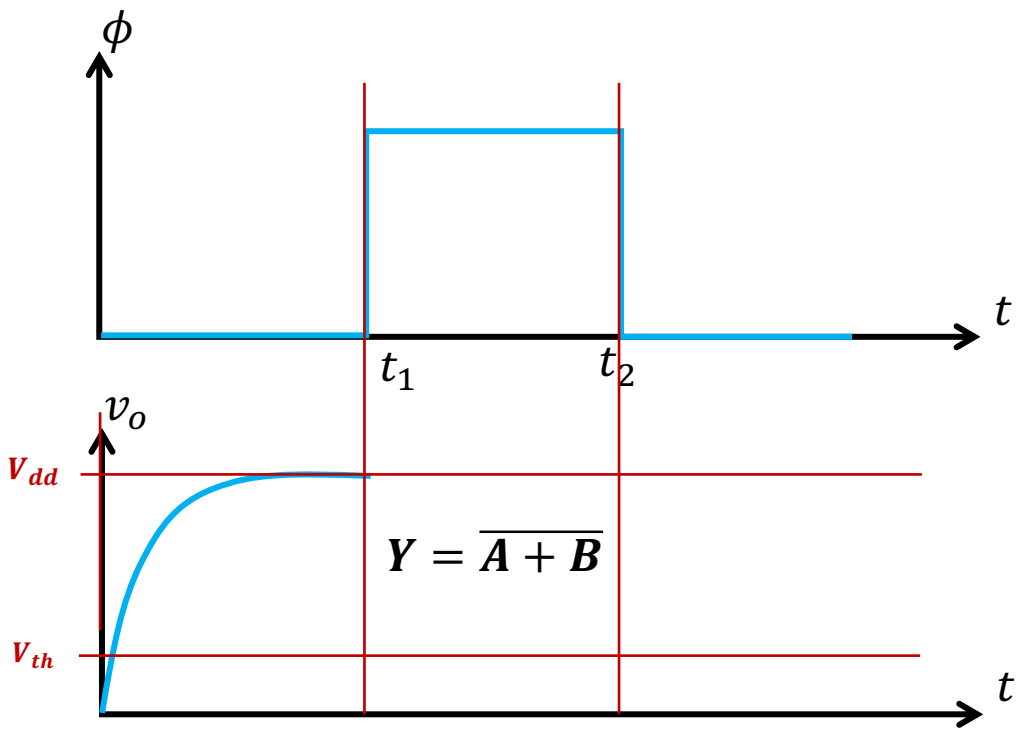
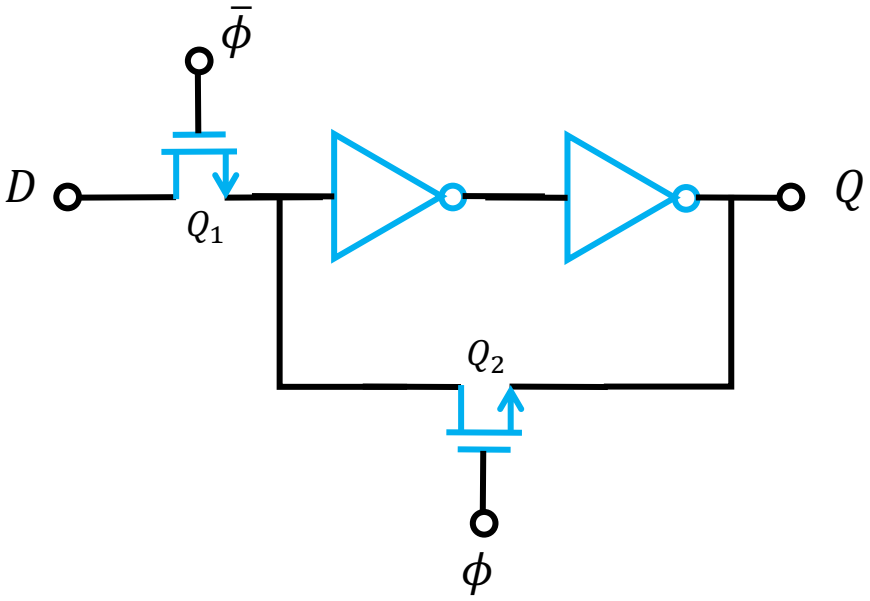
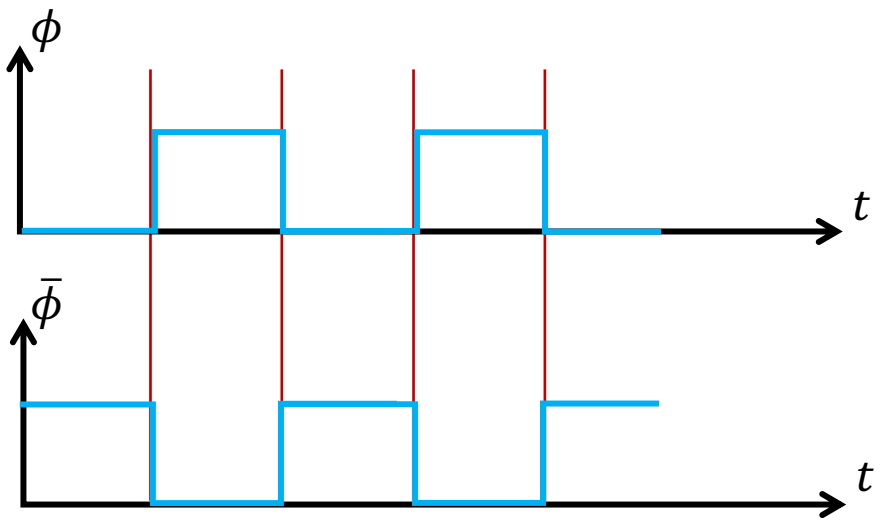




Example 4

QUESTION: Find out the output Q with different input D. ϕ is a clock signal. The input switches between V_{dd} and GND





Example 4

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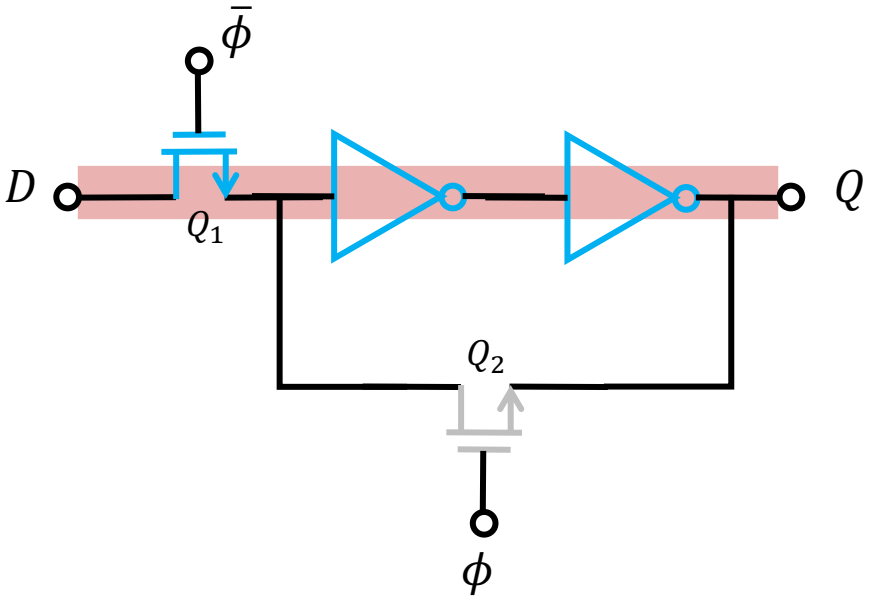
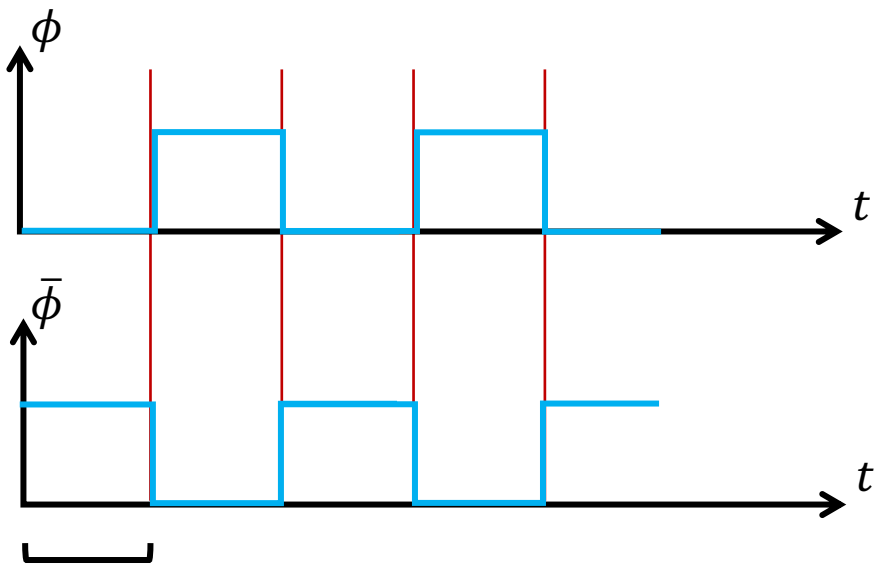




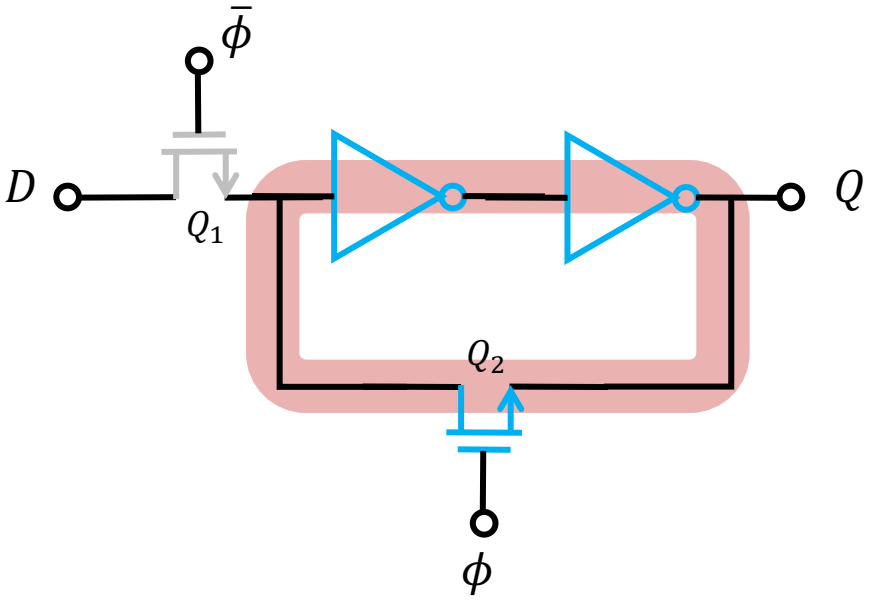
Q_1 is ON

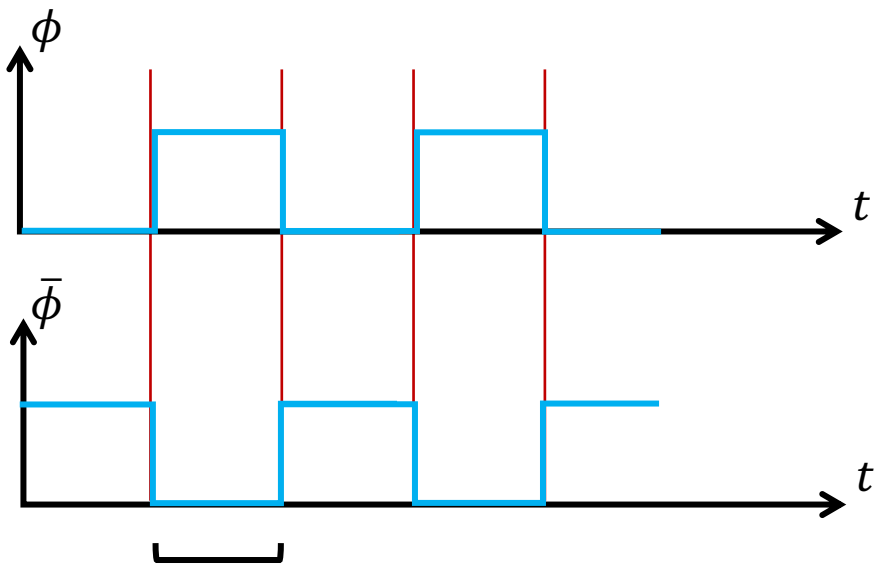
Q_2 is OFF

$\boldsymbol{Q = D}$

Example 4

QUESTION: Find out the output Q with different input D. ϕ is a clock signal. The input switches between V_{dd} and GND

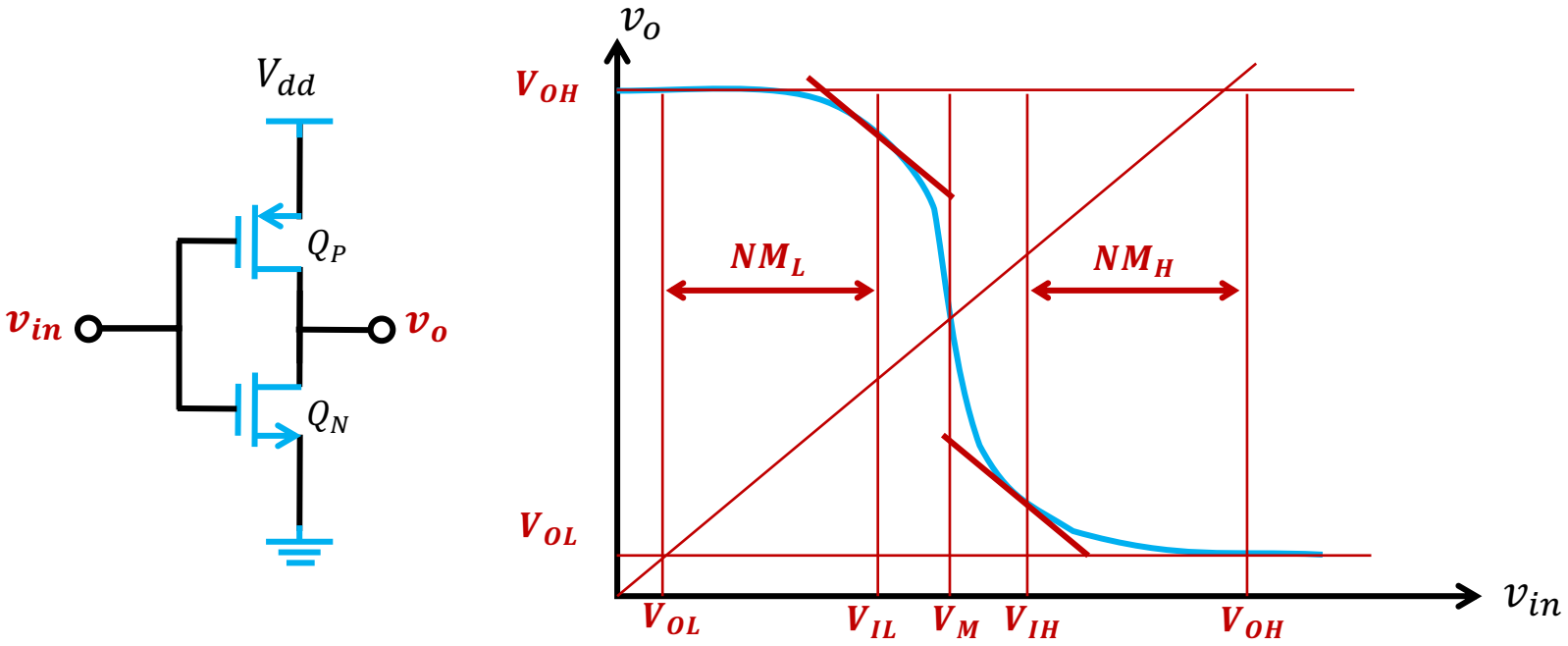




Q_1 is OFF

Q_2 is ON

Recall: VTC of an Invertor



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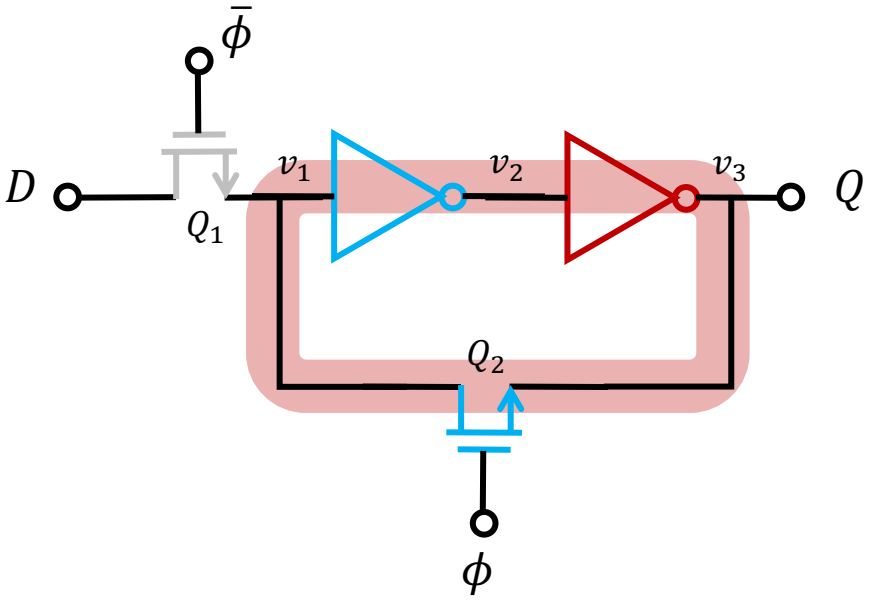

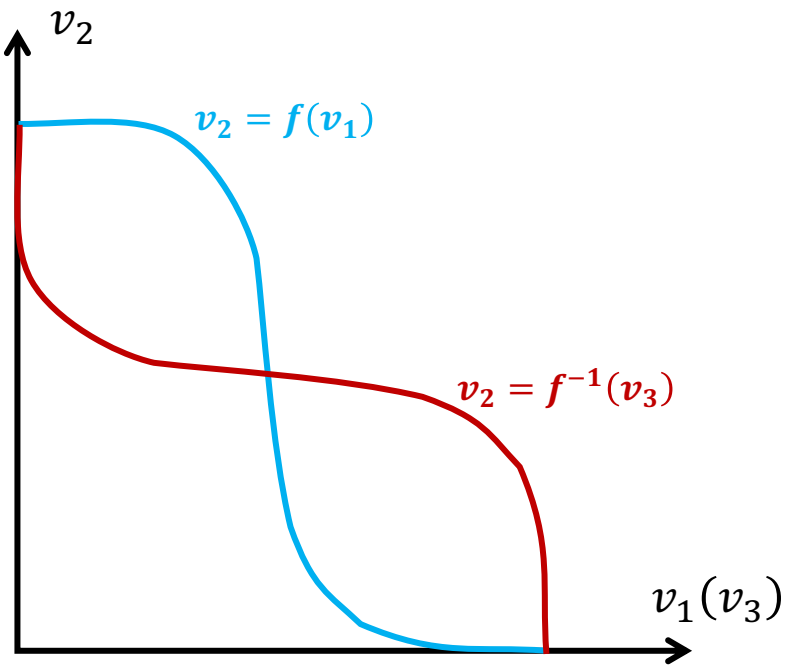

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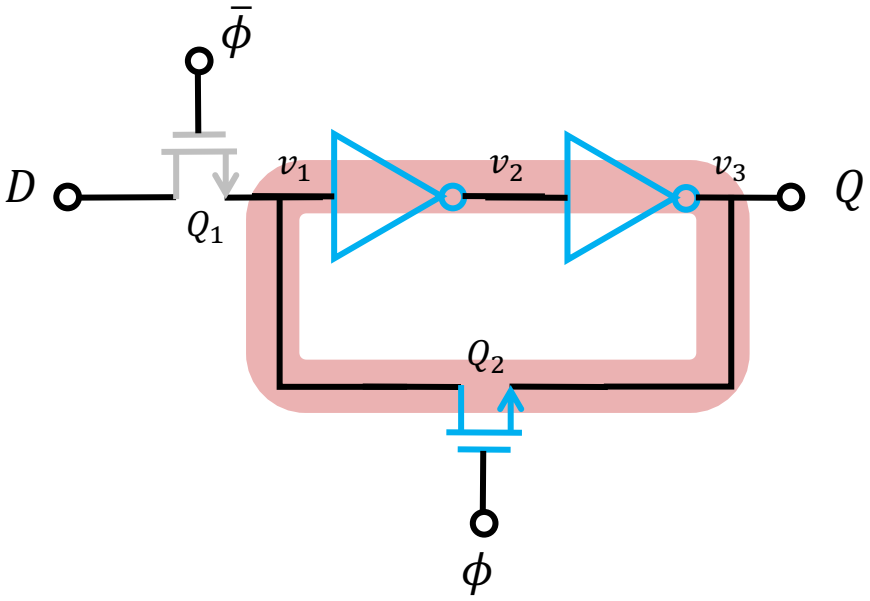

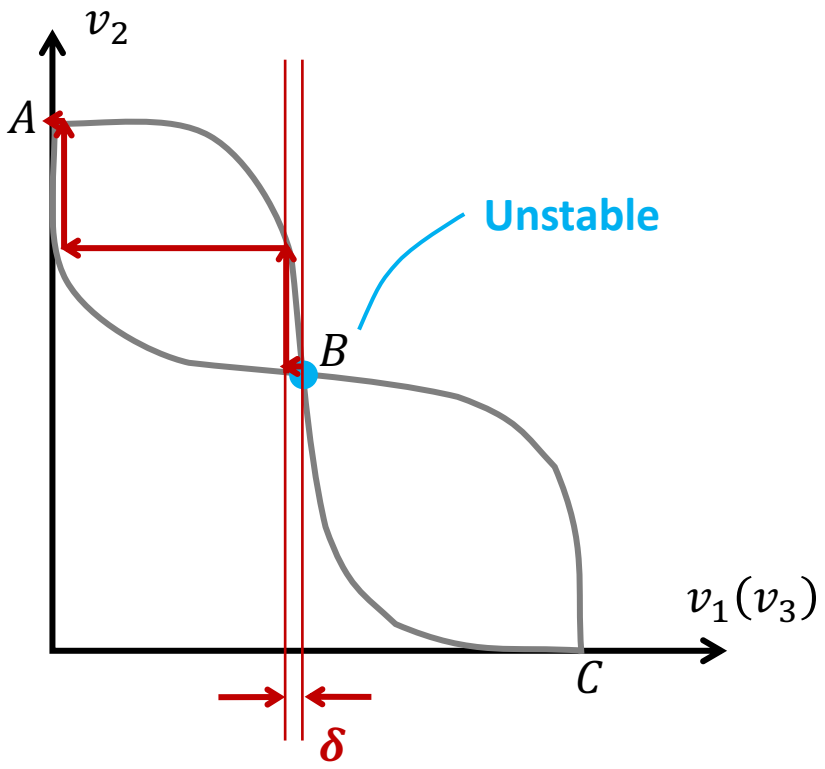

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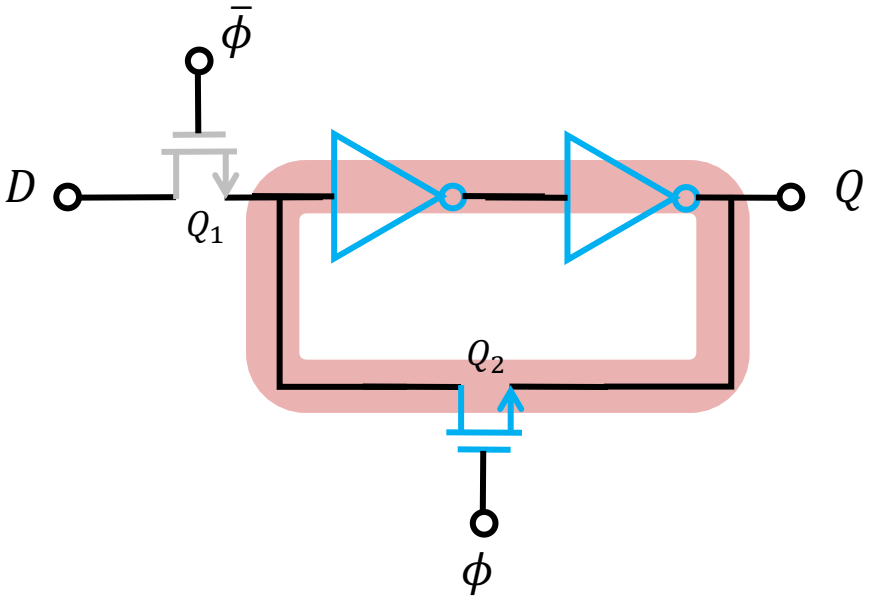
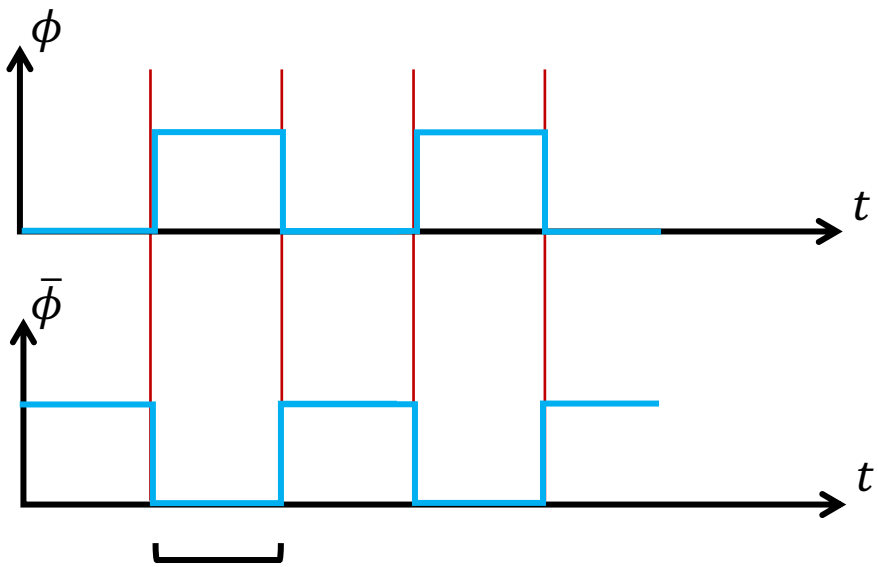




Q_1 is OFF

Q_2 is ON

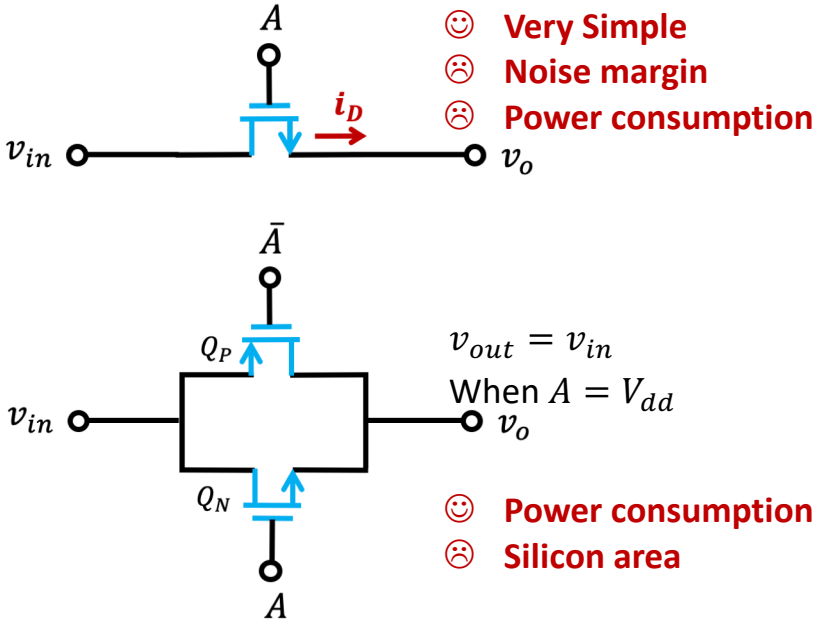
Q does not change

This is a simplest D Flip-Flop

Learn more in 30230793

Outline

- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches &
  Dynamic Logic Circuits
  - Single NMOS switch
  - Transmission Gate Switch
  - Dynamic logic circuits
- **Memory Circuits**



2 Types of Computer Memory

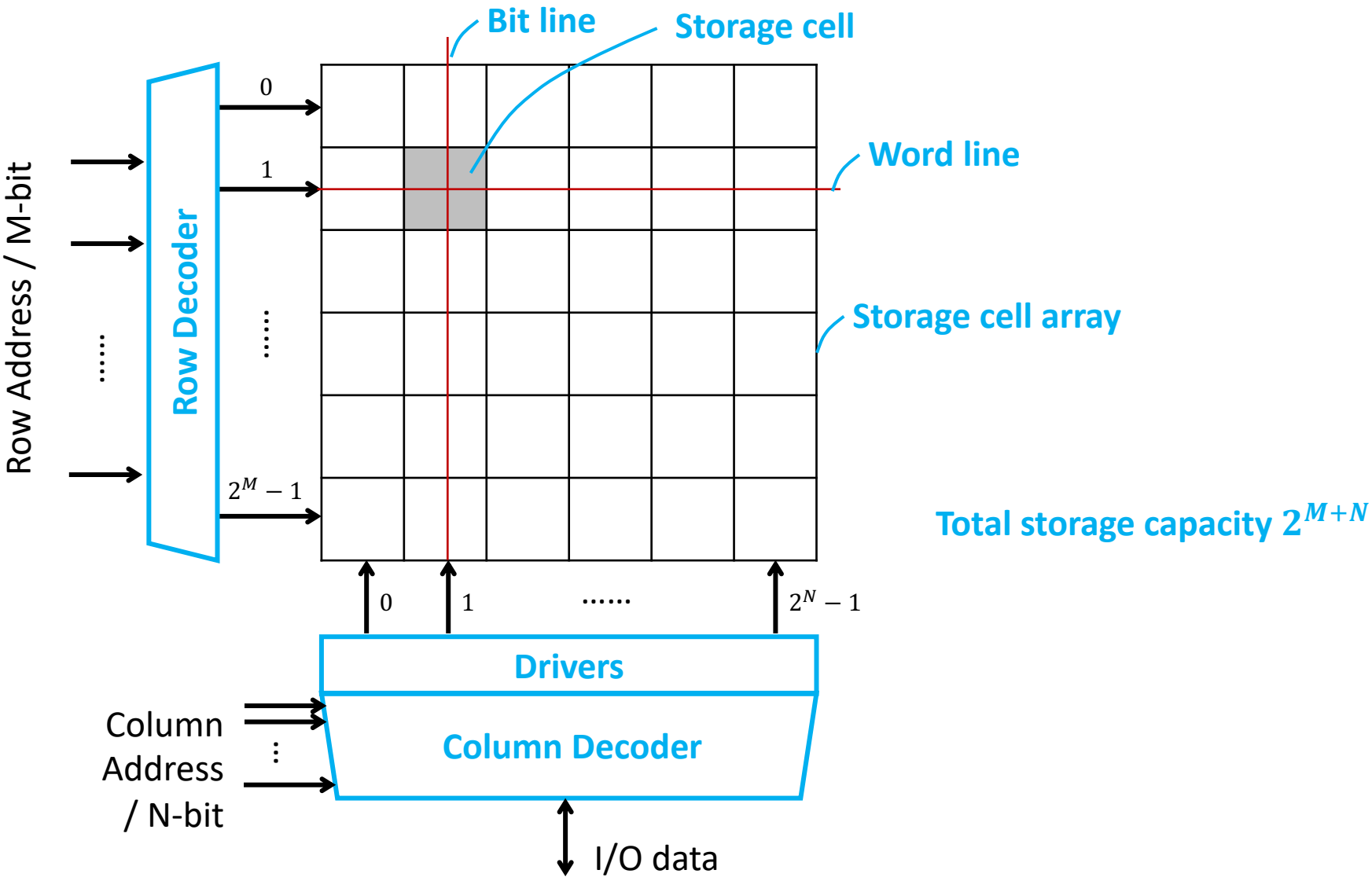
Main memory

- Usually most rapidly accessible
- Usually **random-access**
- Execute most/all instructions

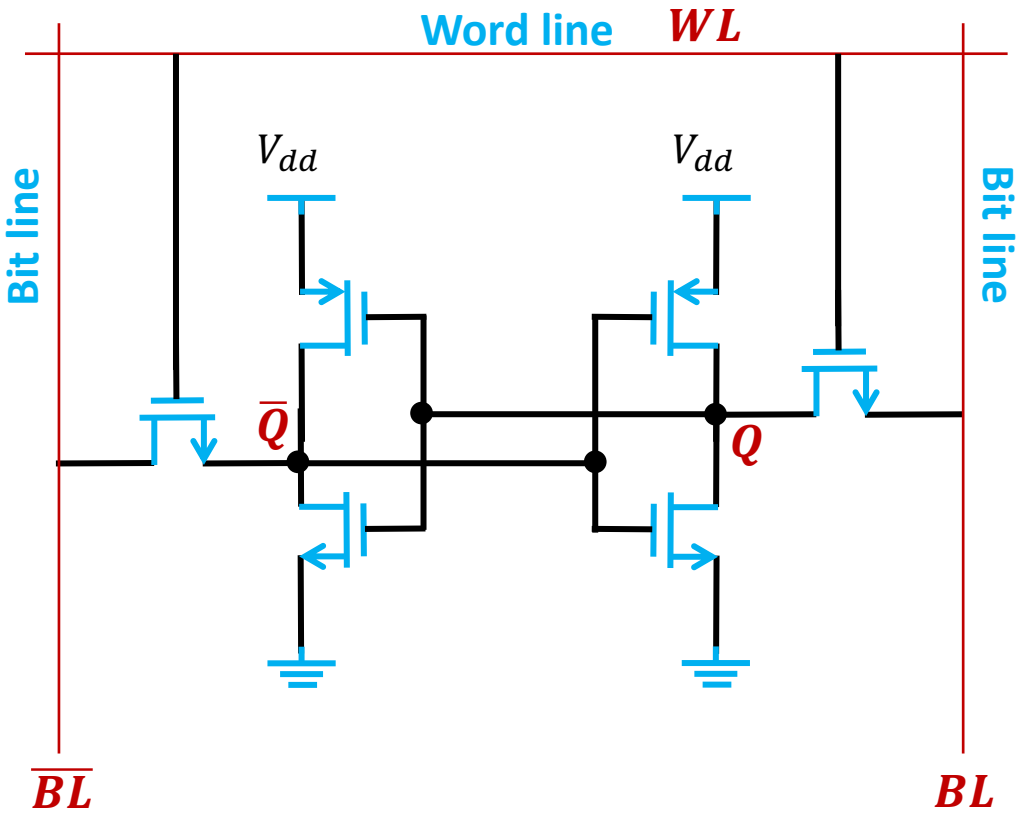
Mass-storage memory

- High storage capability

Random-Access Memory Chip



Random-Access Memory Cell

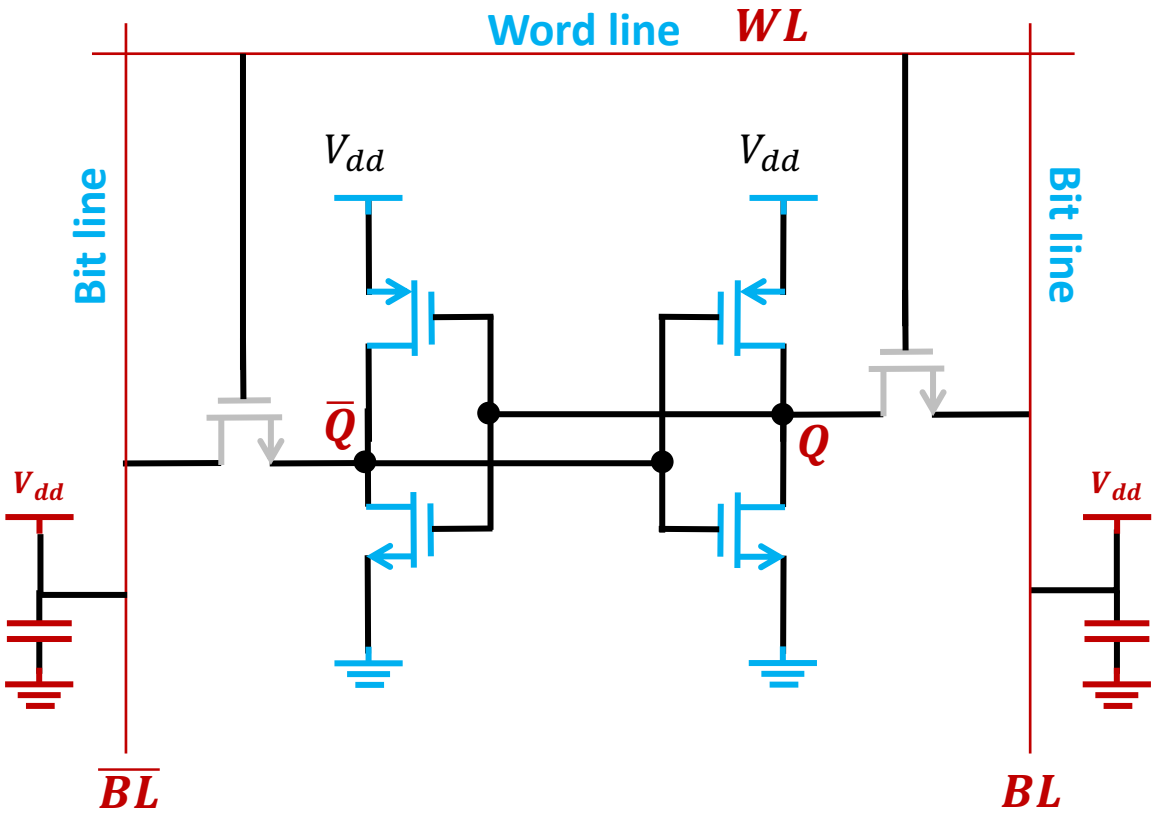


READ OPERATION

- WL is pulled down

Static Random-Access Memory (SRAM) Cell

Random-Access Memory Cell

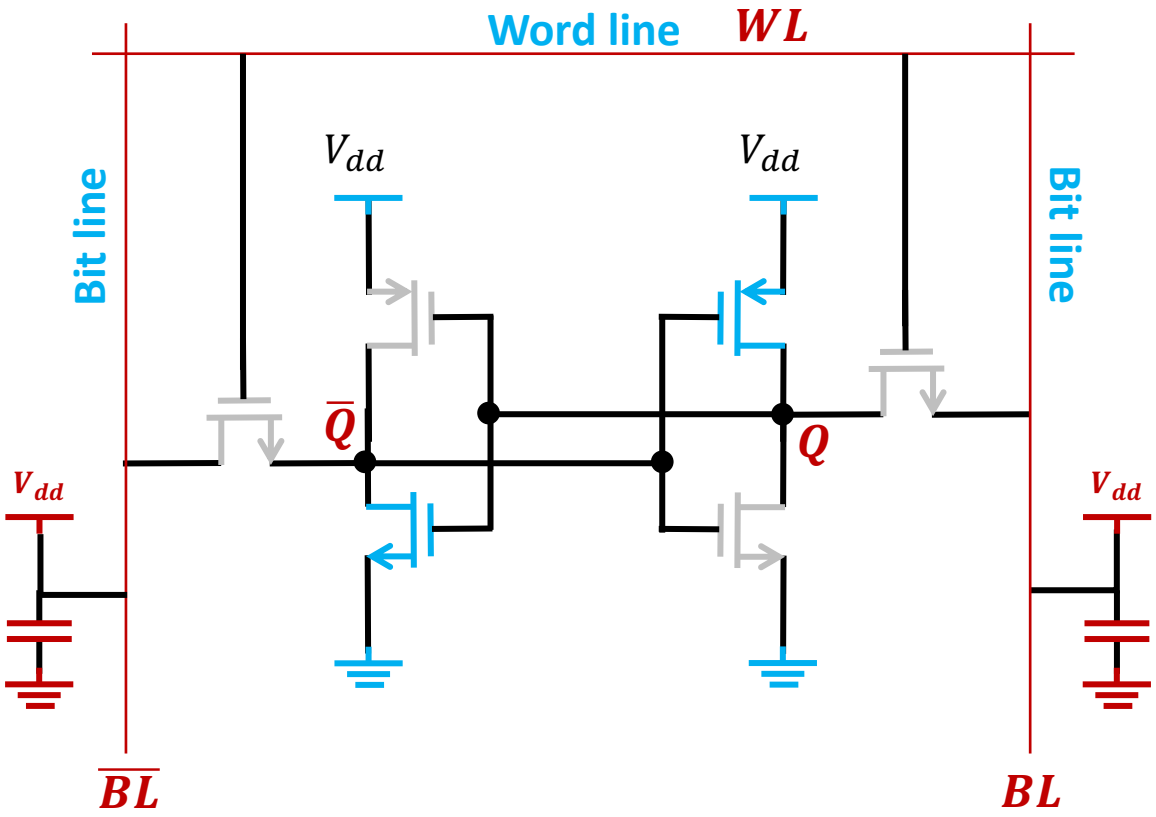


READ OPERATION

- Word line is pulled down
- Bit lines are recharged to V_{dd}

Static Random-Access Memory (SRAM) Cell

Random-Access Memory Cell

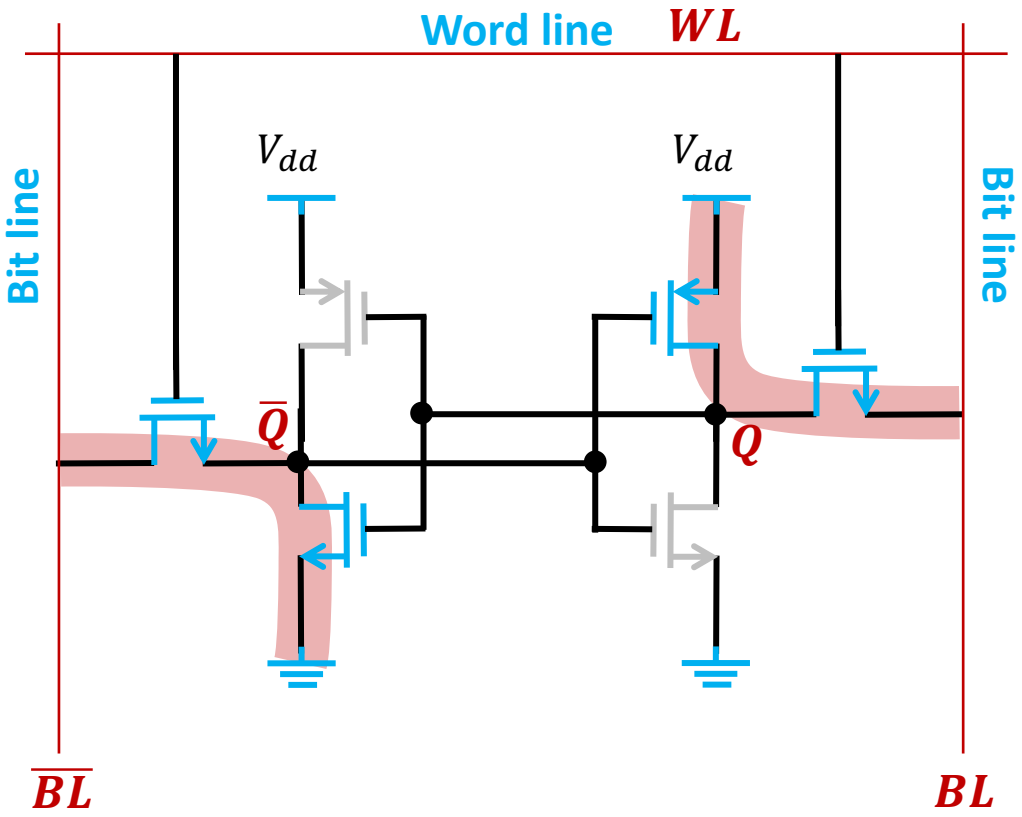


Static Random-Access Memory (SRAM) Cell

READ OPERATION

- Word line is pulled down
- Bit lines are recharged to V_{dd}
- Assume the stored $Q = V_{dd}$

Random-Access Memory Cell

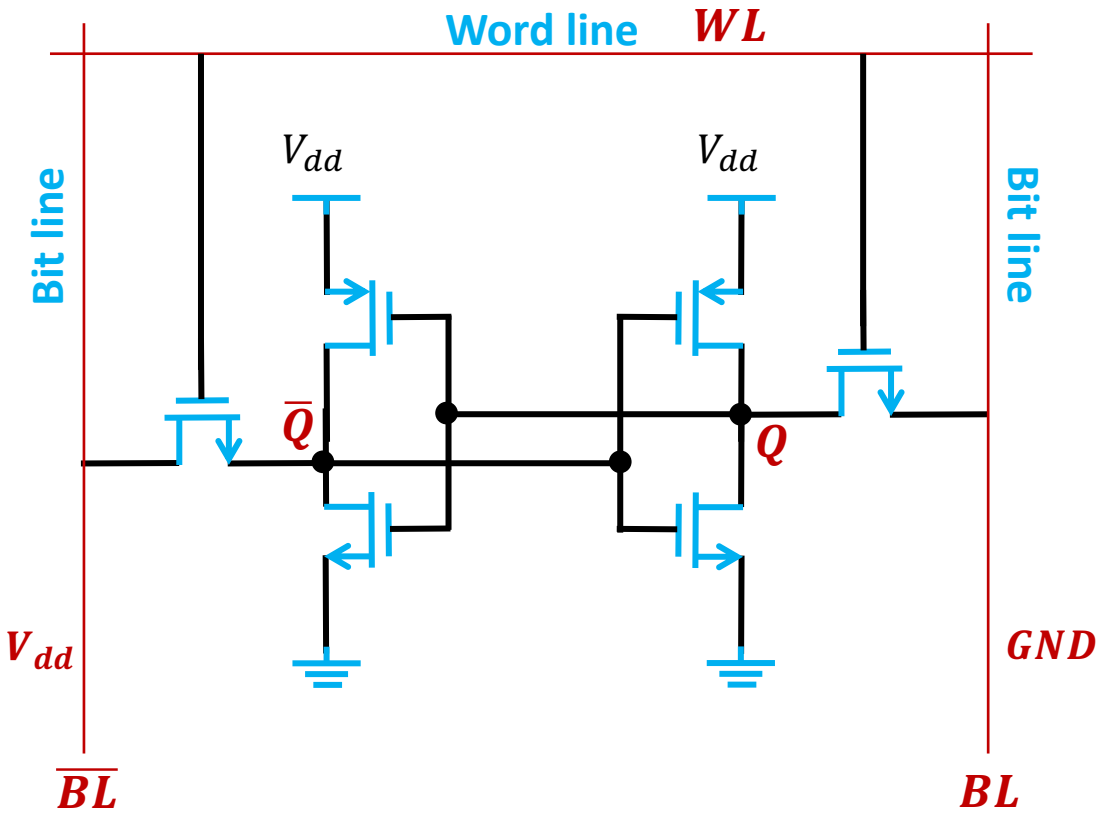


Static Random-Access Memory (SRAM) Cell

READ OPERATION

- Word line is pulled down
- Bit lines are recharged to V_{dd}
- Assume the stored $Q = V_{dd}$
- Pull up the word line
- BL keeps V_{dd}.
- $\overline{BL}$ is pulled down to $\bar{Q}$.

Random-Access Memory Cell

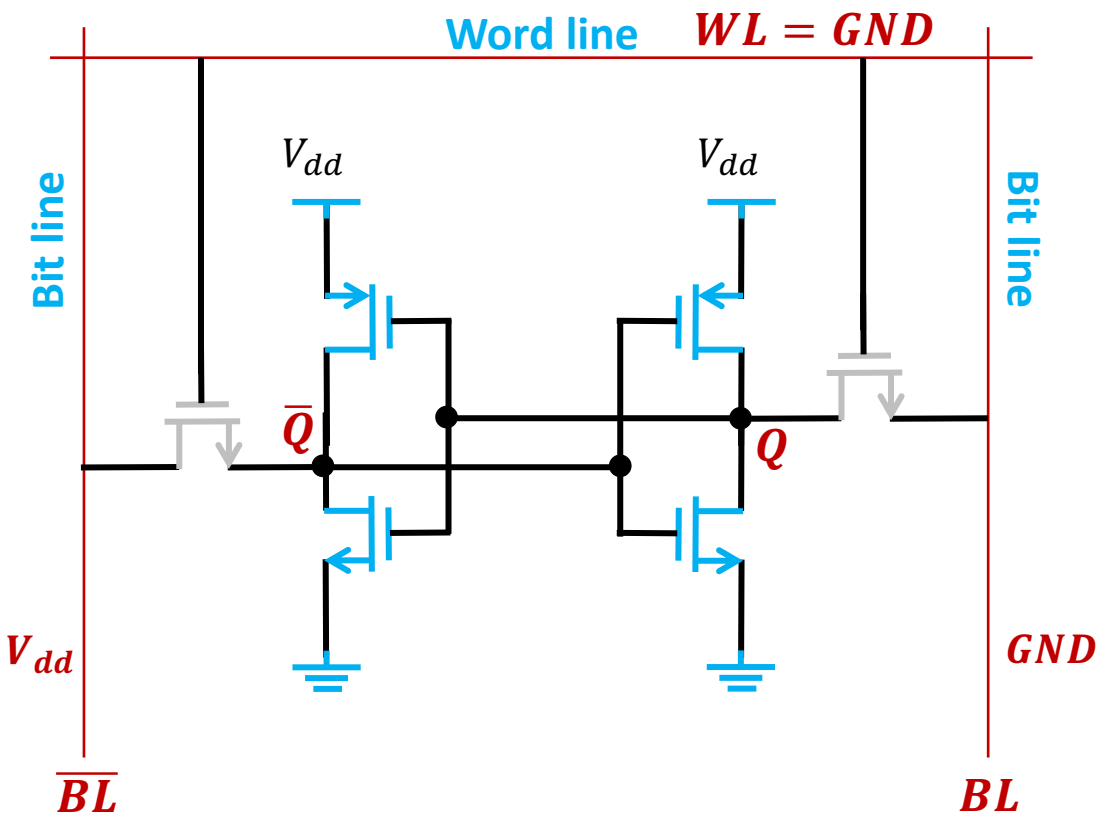


WRITE OPERATION

- Assume the stored $Q = V_{dd}$
- Pull down the word line

Static Random-Access Memory (SRAM) Cell

Random-Access Memory Cell

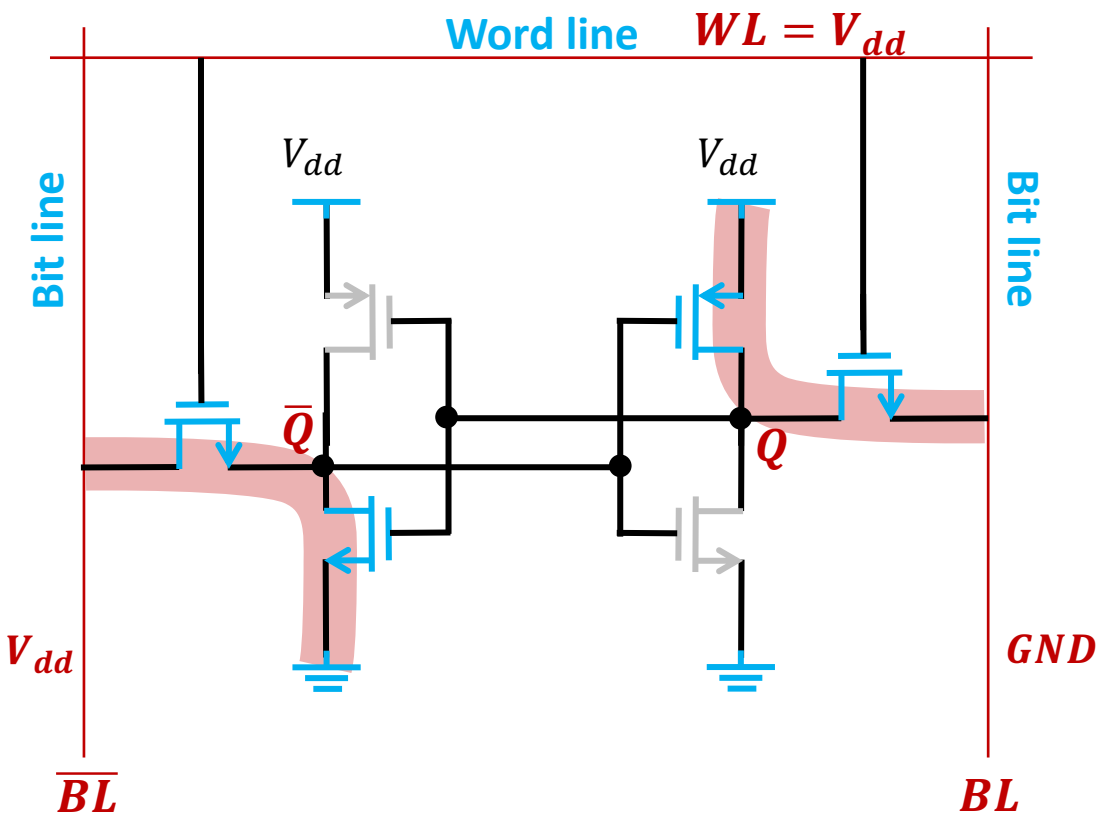


WRITE OPERATION

- Assume the stored $Q = V_{dd}$
- Pull down the word line
- Assume GND is to be written
- Pull down BL to GND
- Pull up $\overline{BL}$ to V_{dd}

Static Random-Access Memory (SRAM) Cell

Random-Access Memory Cell

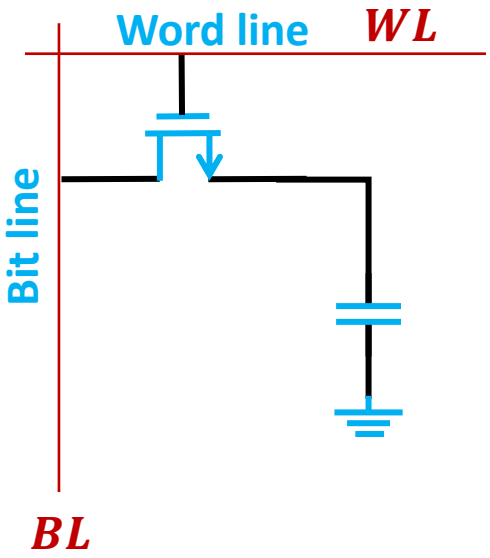


WRITE OPERATION

- Assume the stored $Q = V_{dd}$
- Pull down the word line
- Assume GND is to be written
- Pull down BL to GND
- Pull up $\overline{BL}$ to V_{dd}
- The word line is pull up
- $\bar{Q}$ is pull up to V_{dd}
- Q is discharged to GND

Static Random-Access Memory (SRAM) Cell

Random-Access Memory Cell



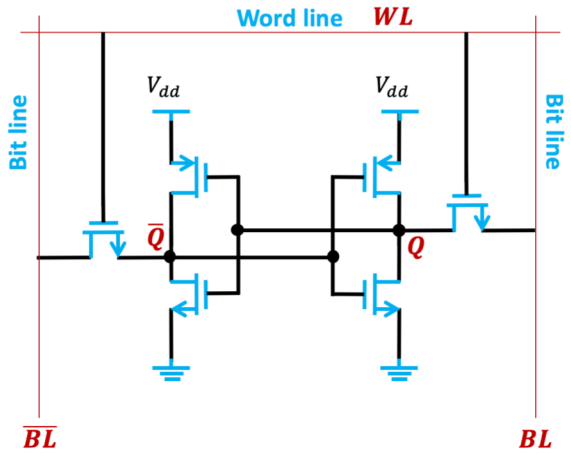
Dynamic Random-Access Memory (DRAM) Cell

WRITE OPERATION

- Assume the stored $Q = GND$
- Pull down the word line
- Assume V_{dd} is to be written
- Pull up BL to V_{dd}
- The word line is pull up
- Q is charged to $V_{dd} - V_{th}$

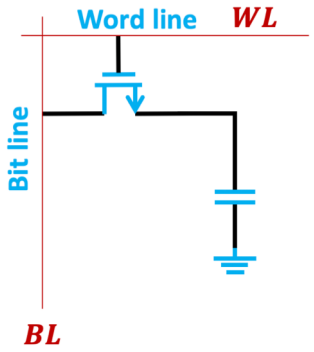
Summary: Random-Access Memory

Static RAM (SRAM) Cell



- Data stored in **latches**
- Simple **read/write operation**
- Relative large **area**

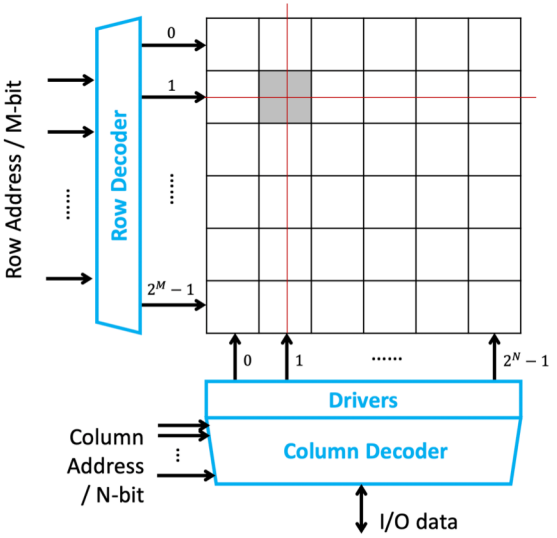
Dynamic RAM (DRAM) Cell

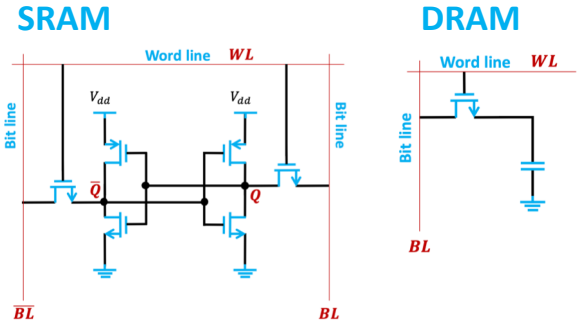


- Data stored in **capacitors**
- Complex **read/write operation**
- Low silicon **area** consumption

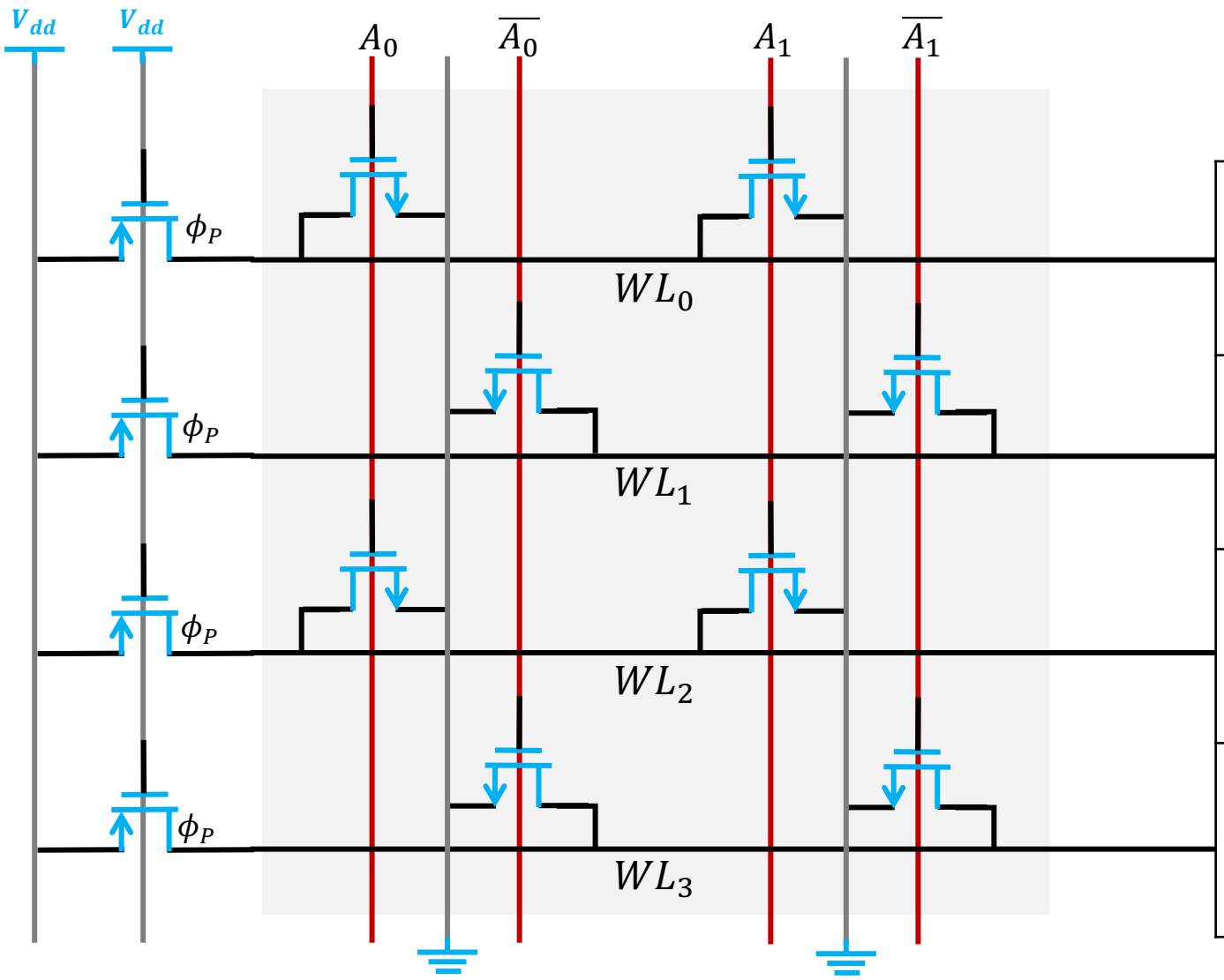
Outline

- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches & Dynamic Logic Circuits
- Memory Circuits
  - Overview
  - Memory cell
  - **Address decoder**



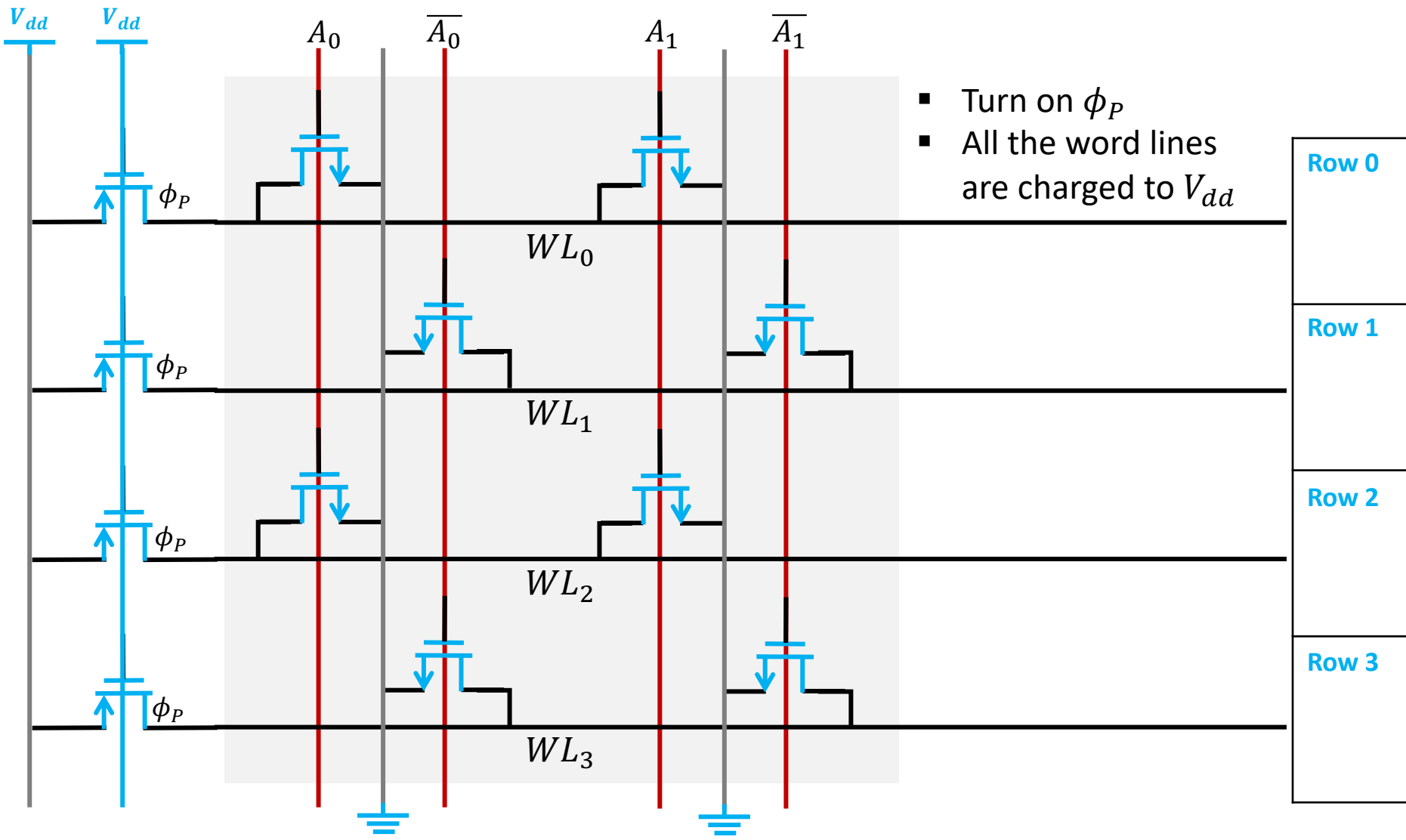


Row-Address Decoder



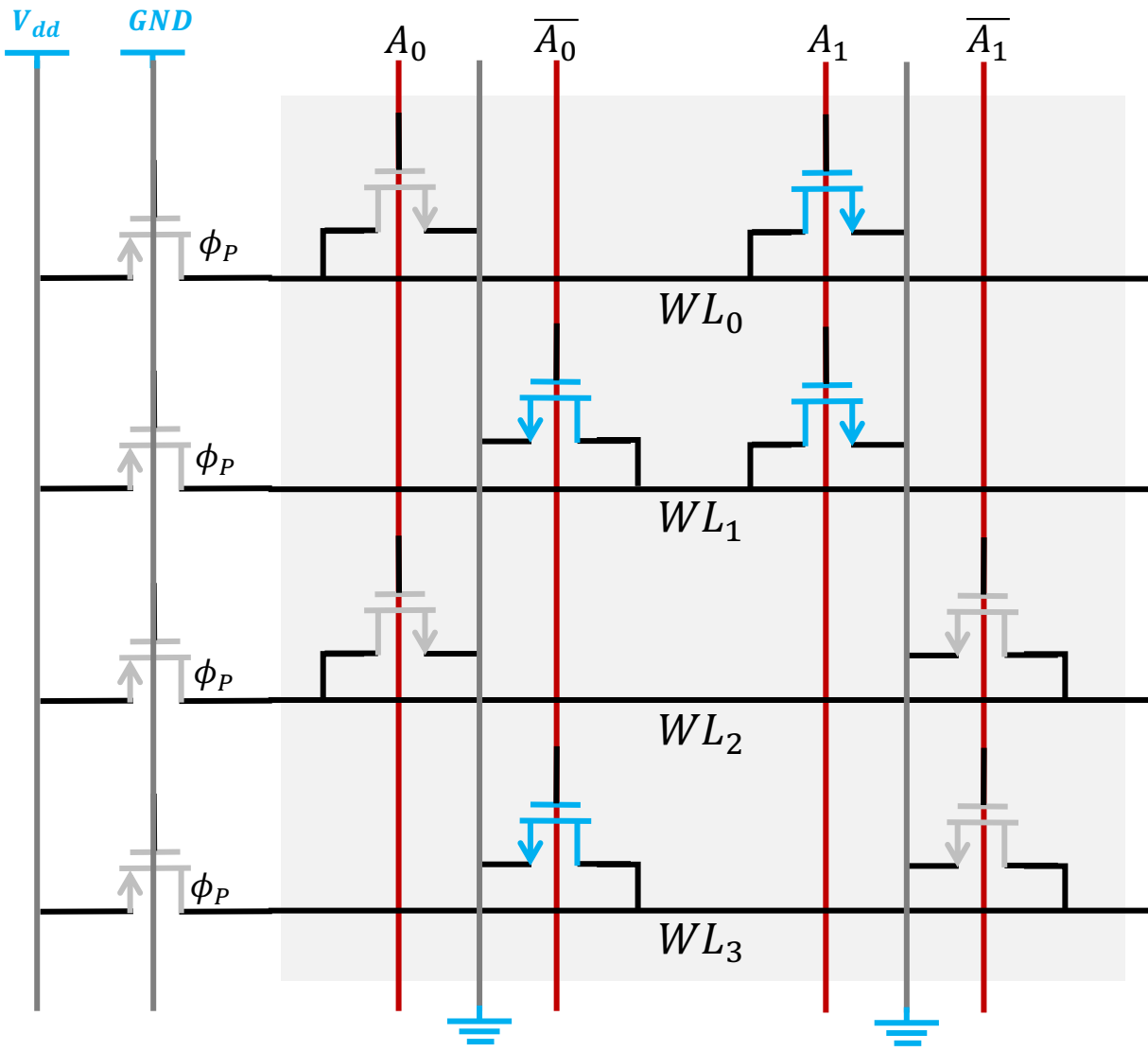
Row 0	
Row 1	
Row 2	
Row 3	

Row-Address Decoder



- Turn on ϕ_P
- All the word lines are charged to V_{dd}

Row-Address Decoder



- Turn on ϕ_P
- All the word lines are charged to V_{dd}

- Turn off ϕ_P
- If $A_1A_0 = 10$

- WL_0, WL_1, and WL_3 are discharged
- Only WL_2 keeps V_{dd}

Row 0

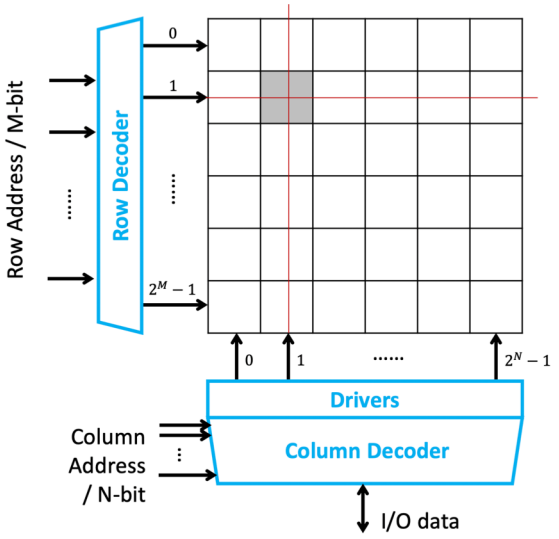
Row 1

Row 2

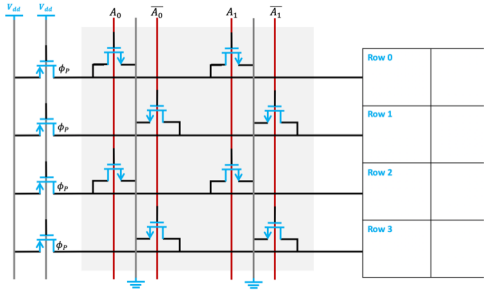
Row 3

Outline

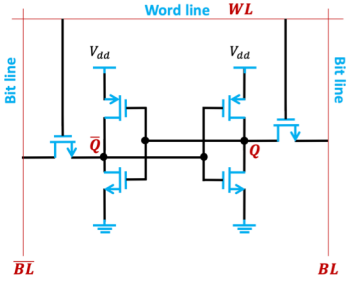
- CMOS Inverters
- Logic-Gate Circuits
- Digital Switches & Dynamic Logic Circuits
- Memory Circuits
  - Overview
  - Memory cell
  - Address decoder



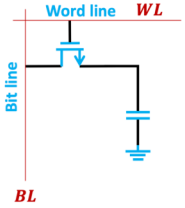
Address decoder



SRAM



DRAM



Reading tasks & learning goals

- Reading tasks
  - Microelectronic Circuits, 6th edition
    - Chapter 13 – 14.3.1, 15.2 – 15.3, 15.4.2
- Learning goals
  - Well understand how to analyze the **power consumption**, **propagation delay** and **noise margins** of a CMOS logic gate
  - Well understand how to analyze the **logic-gate circuits**
  - Well understand how to analyze the **CMOS switch circuit**
  - Know the different types of **memory** circuits