

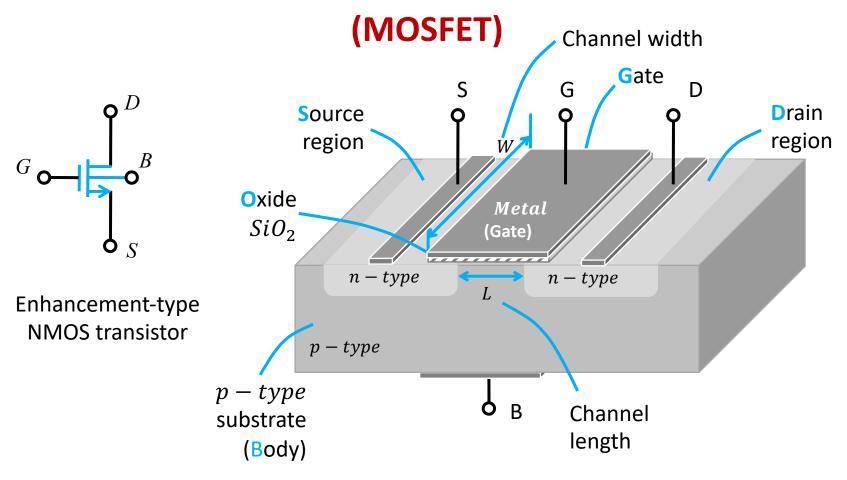
MOS Field-Effect Transistors

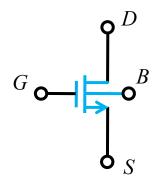
Milin Zhang Dept of EE, Tsinghua University

Outline

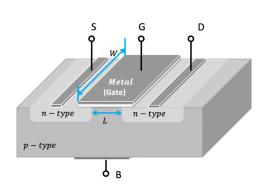
- Introduction to MOSFET
 - WHAT does it look like
 - HOW does it work
- The characteristic curves
- Circuit analysis techniques with MOSFET
- MOSFET v.s. BJT
- More examples of useful modules

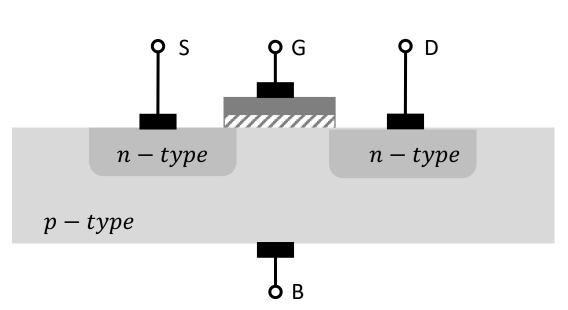
Metal-Oxide-Semiconductor Field-Effect Transistors



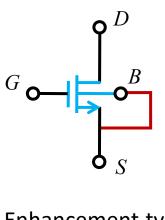


Enhancement-type NMOS transistor



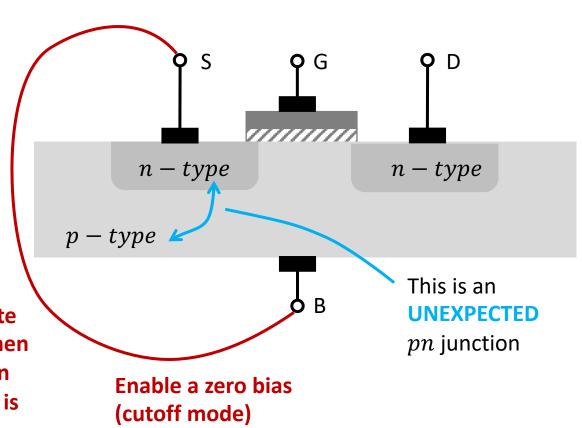


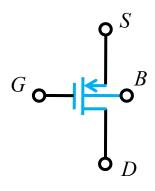
Cross section of an enhancement-type NMOS transistor



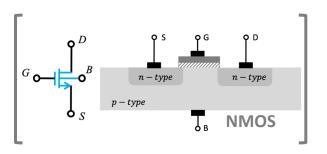
Enhancement-type NMOS transistor

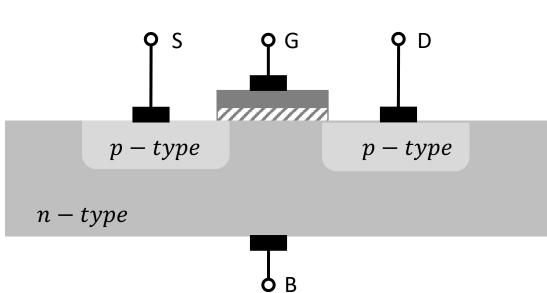
Body effect: the substrate acts as a second gate when the pn junction between the base and the source is forward biased





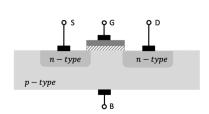
Enhancement-type PMOS transistor



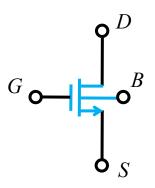


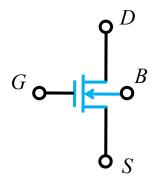
Cross section of an enhancement-type PMOS transistor

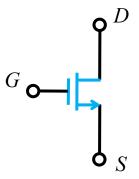
Circuit symbols of MOSFET

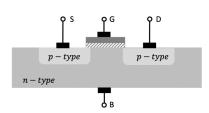


Enhancement-type NMOS transistor

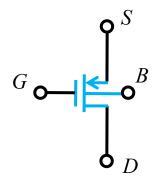


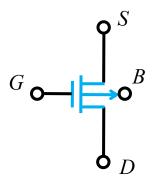


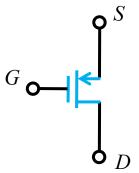




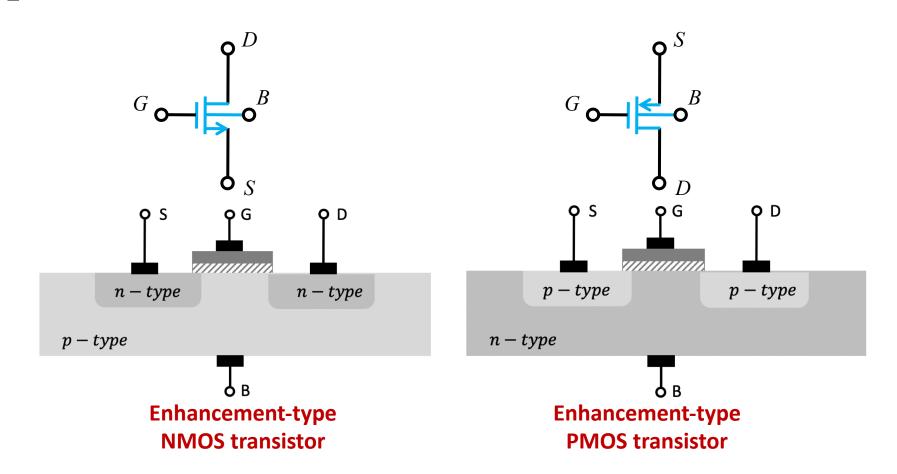
Enhancement-type PMOS transistor





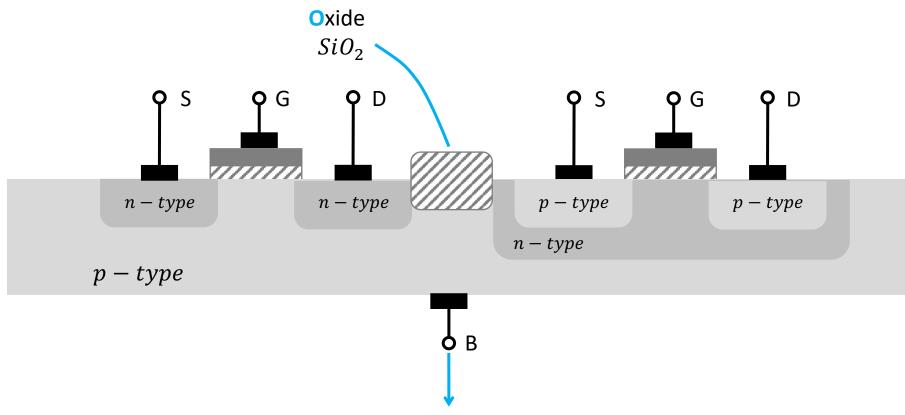


NMOS v.s. PMOS



How to integrate NMOS & PMOS onto a same substrate?

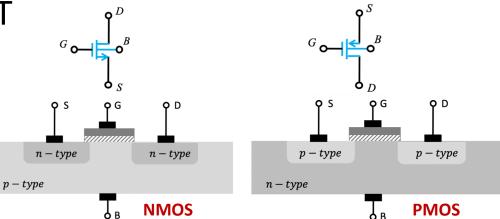
Complementary MOS (CMOS)

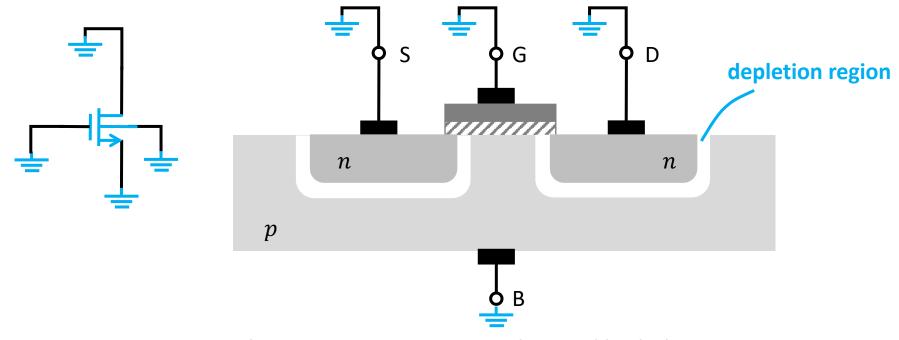


Connected to the most negative power supply to avoid body-effect

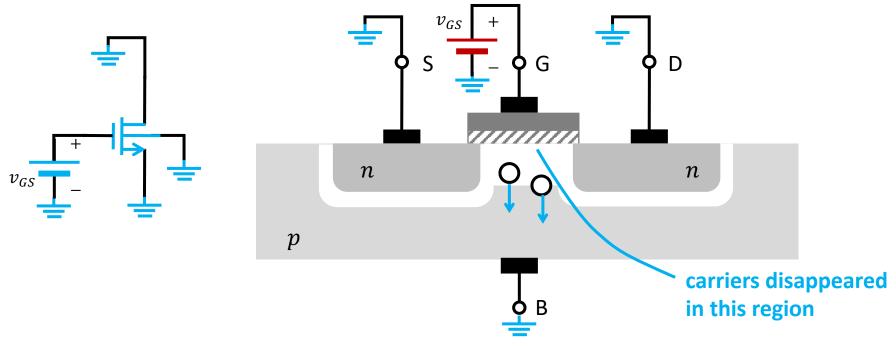
Outline

- Introduction to MOSFET
 - WHAT does it look like
 - HOW does it work

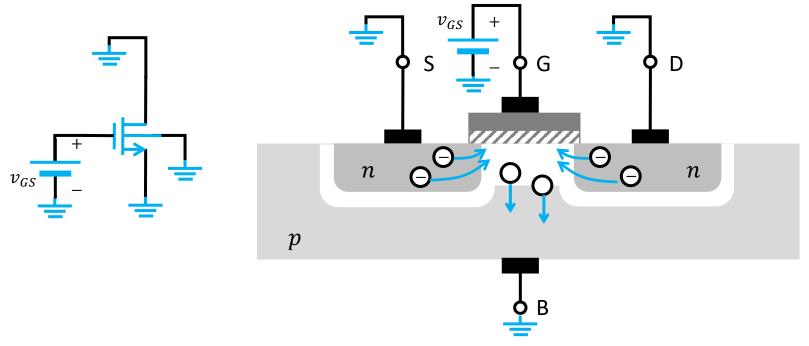




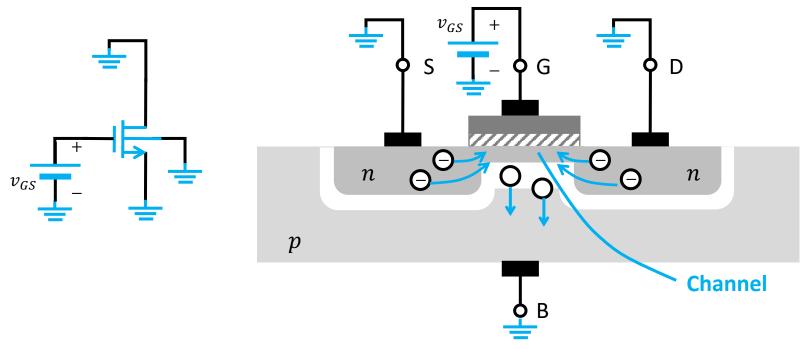
 Depletion regions are generated around both the Source and the Drain



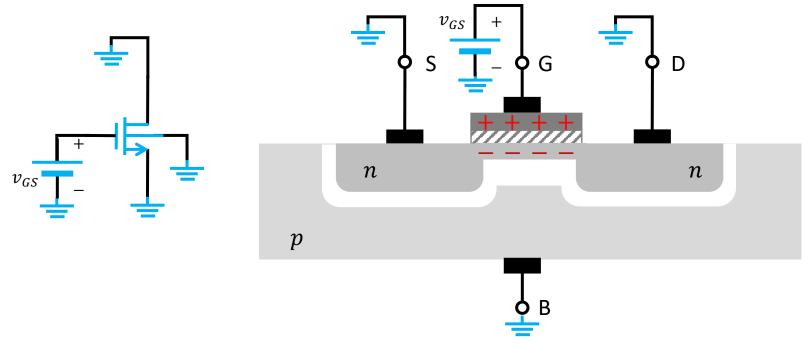
- Apply a voltage v_{GS} to the gate
- The holes are pushed downward into the substrate



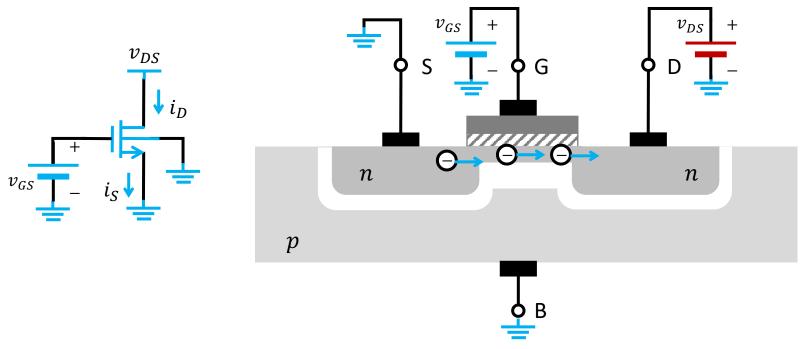
 The electrons from source and drain are attracted into the "carrier-disappeared" region



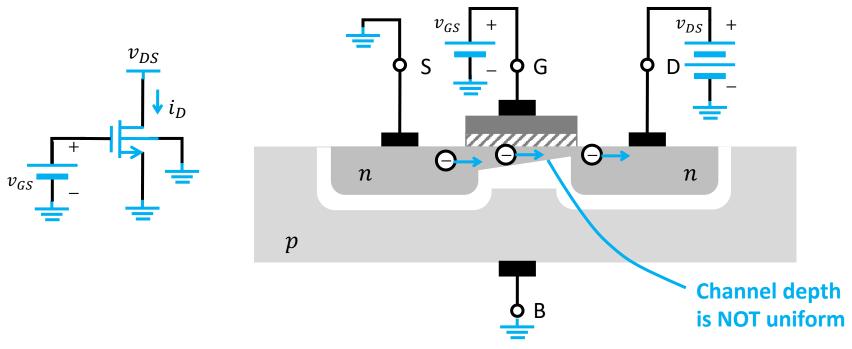
- The induced electrons forms a n type channel
- this type of MOSFET is called n channel MOSTFET



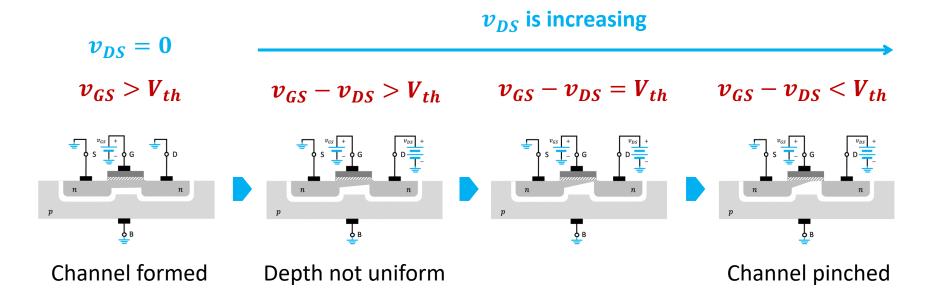
• The gate and the channel region form a parallel-plate capacitor C_{ox} , with the oxide layer acting as the capacitor dielectric



- Apply a small voltage v_{DS} to the gate
- When v_{DS} is higher than the threshold voltage v_{th} , A current i_D flows through the channel
- Currents through the drain and source are the same $i_D = i_S$
- No current @ Gate $i_G = 0$

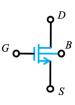


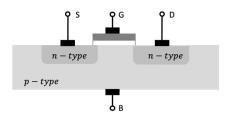
- When the voltage v_{DS} is increased
- The voltage difference $v_{GS}\gg v_{GD}=v_{GS}-v_{DS}$
- Channel is NOT uniform depth



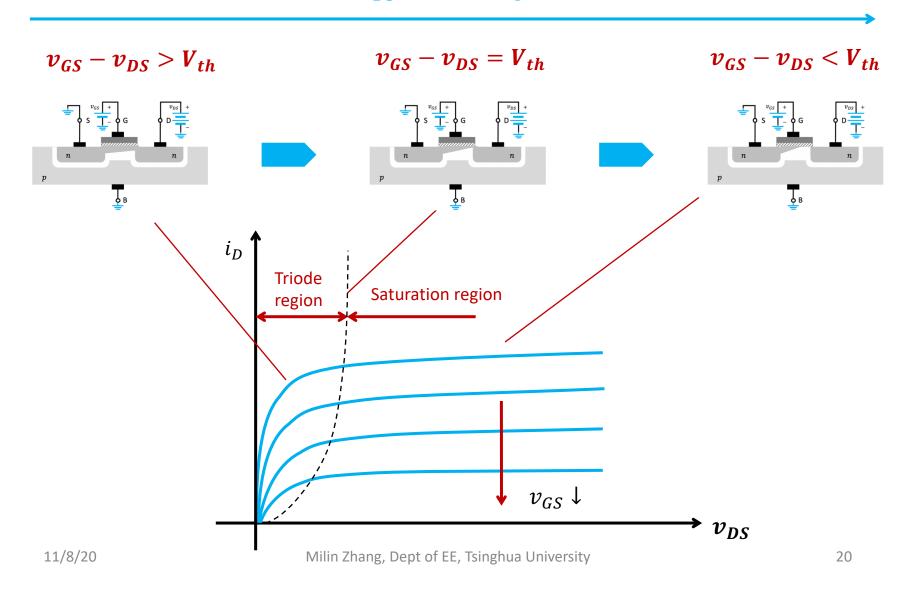
Outline

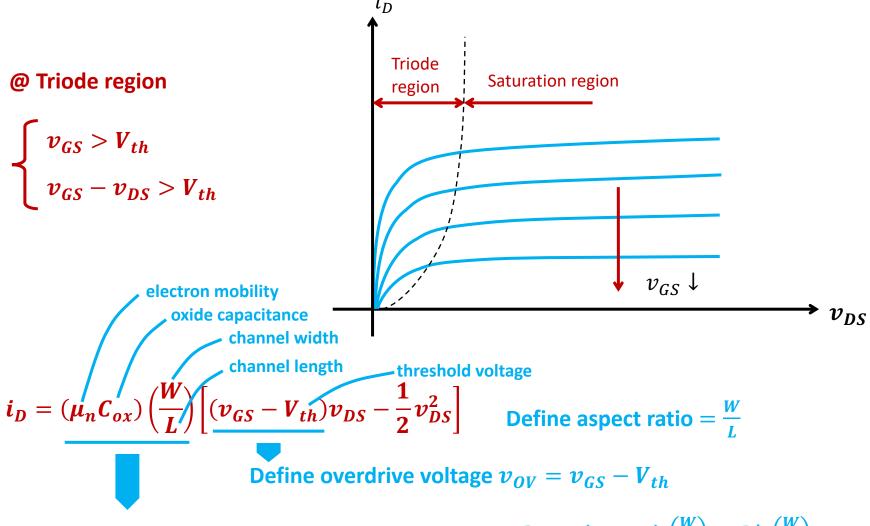
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- The characteristic curves



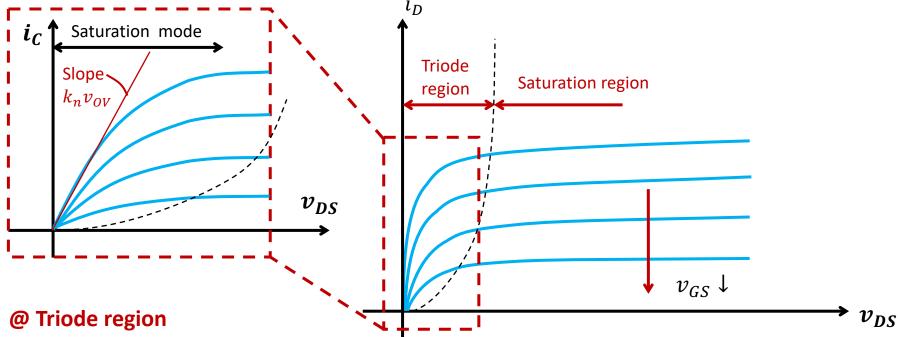


v_{DS} is increasing





Define MOSFET transconductance parameter $k_n = (\mu_n C_{ox}) \left(\frac{w}{L} \right) = k_n' \left(\frac{w}{L} \right)$



$$\begin{split} i_D &= k_n \left[(v_{GS} - V_{th}) v_{DS} - \frac{1}{2} v_{DS}^2 \right] \\ \downarrow &\text{If } v_{DS} \rightarrow 0 \\ &\approx k_n (v_{GS} - V_{th}) v_{DS} \end{split}$$

MOSFET behaves as a linear resistance r_{DS} when v_{DS} kept small

Define
$$r_{DS} = rac{1}{k_n(v_{GS} - V_{th})} = rac{1}{k_n v_{OV}}$$

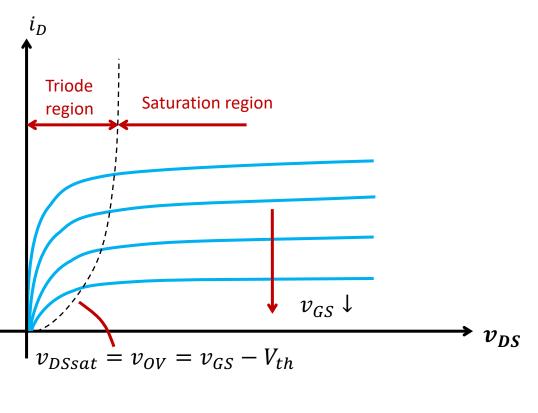
@ boundary between regions

$$\begin{cases} v_{GS} > V_{th} \\ v_{GS} - v_{DS} = V_{th} \end{cases}$$

$$i_D = k_n \left[(v_{GS} - V_{th}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$

$$v_{DSsat} = v_{oV}$$

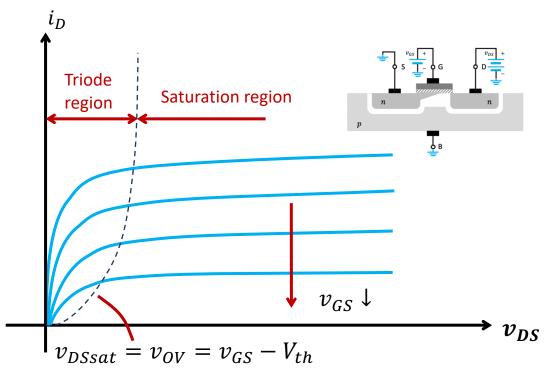
$$= \frac{1}{2} k_n (v_{GS} - V_{th})^2$$



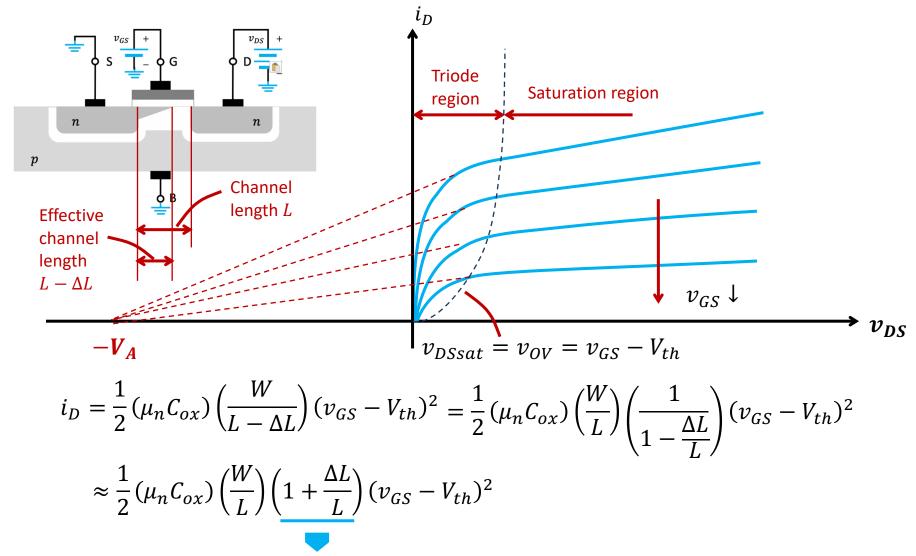
@ Saturation region

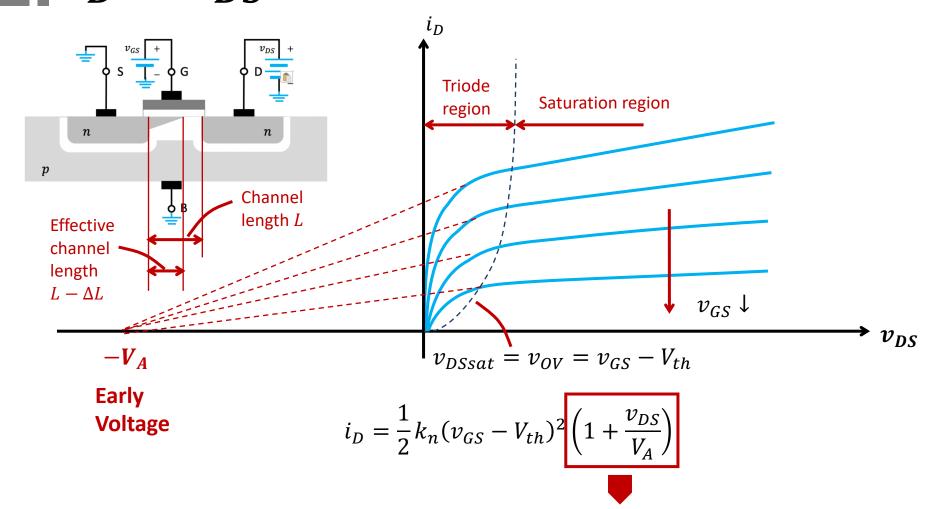
$$\begin{cases} v_{GS} > V_{th} \\ v_{GS} - v_{DS} < V_{th} \end{cases}$$

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{th})^2$$



Current saturates since the channel is pinched off



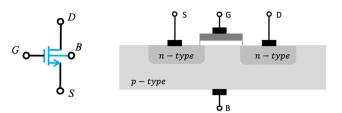


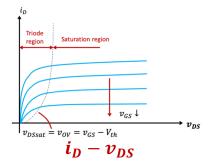
Channel-length modulation (THE EARLY EFFECT)

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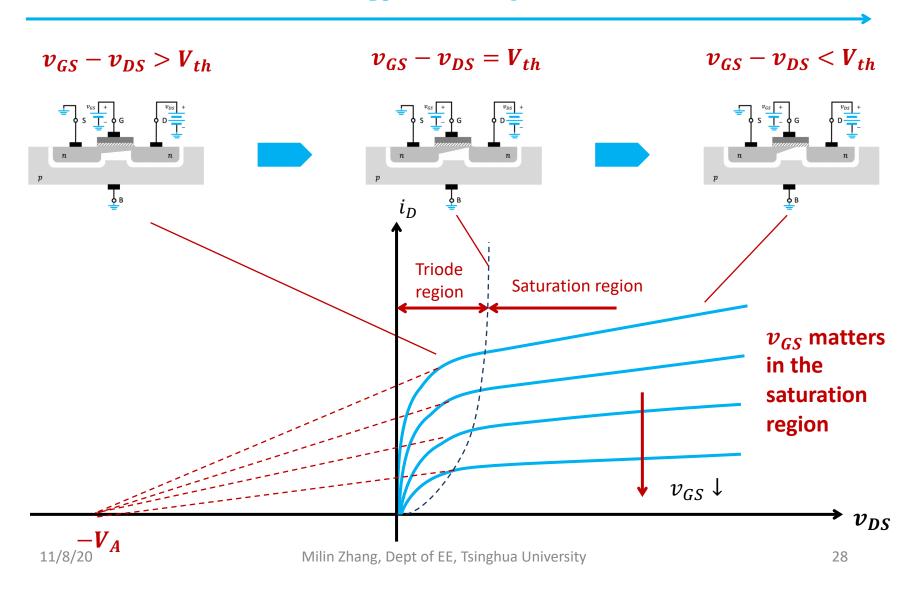
 - $"i_D v_{GS}$ characteristics





Recall: $i_D - v_{DS}$ characteristics

 v_{DS} is increasing

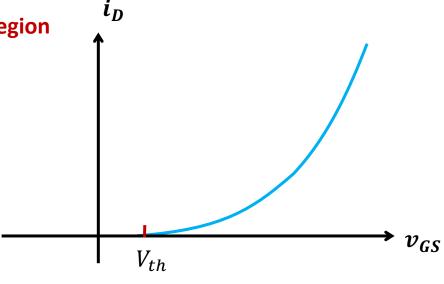


 $v_{\it GS}$ matters in the saturation region

@ Saturation region

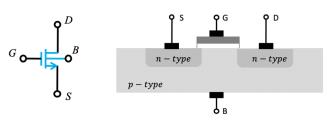
$$\left\{egin{array}{l} v_{GS} > V_{th} \ v_{GS} - v_{DS} < V_{th} \end{array}
ight.$$

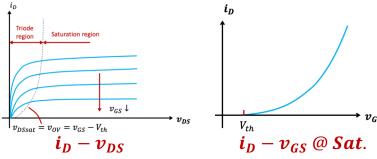
$$i_D = \frac{1}{2} k_n (v_{GS} - V_{th})^2$$

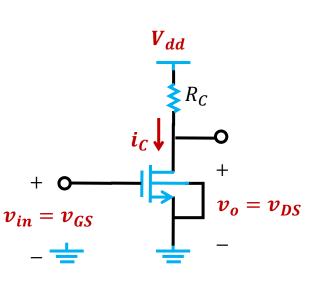


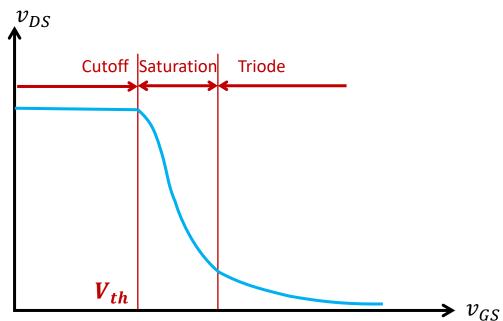
Outline

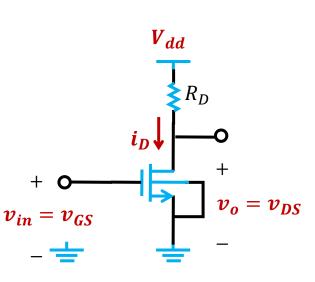
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 - $"i_D v_{GS}$ characteristics
 - The transfer characteristic

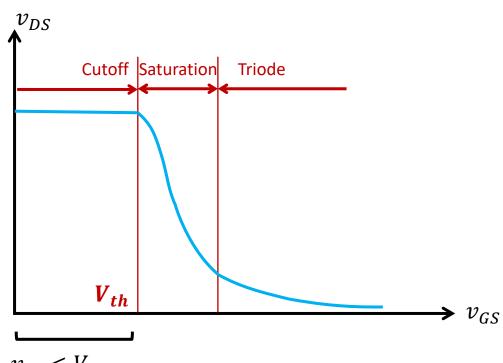








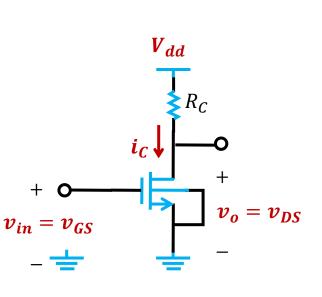


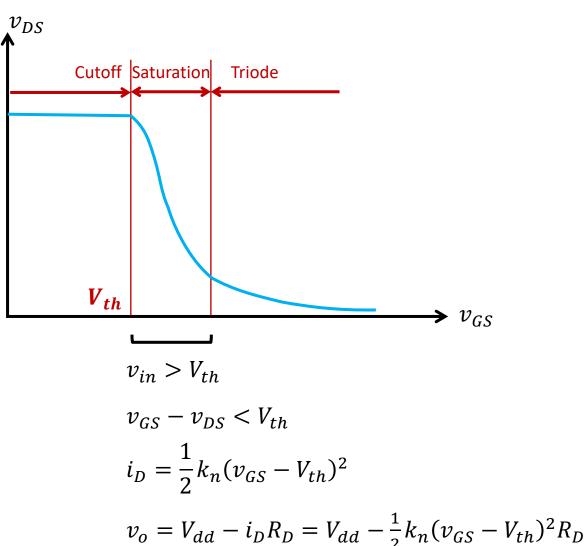


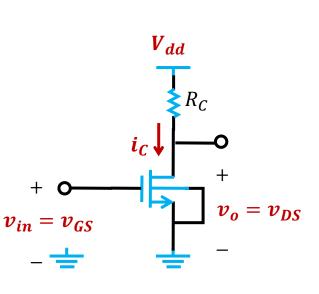
$$v_{in} < V_{th}$$

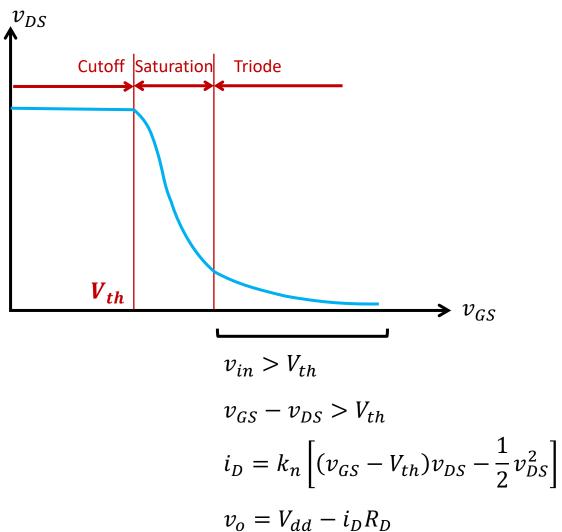
$$i_D = 0$$

$$v_o = V_{dd} - i_D R_D = V_{dd}$$









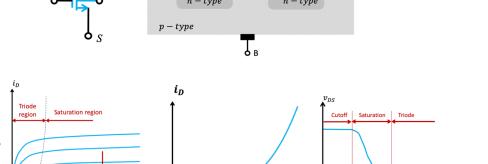
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$$v_D = v_{DS}$$
 characteristics

$$v_D - v_{GS}$$
 characteristics

The transfer characteristic



 $i_D - v_{GS} @ Sat.$

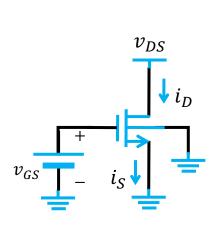
- Circuit analysis techniques with MOSFET
 - DC analysis techniques

 $v_{DSsat} = v_{OV} = v_{GS} - V_{th}$

 $i_D - v_{DS}$

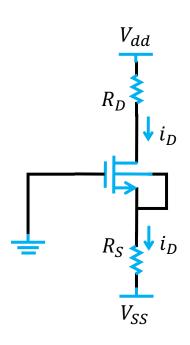
Transfer characteristic

Characteristics Summary of MOSFET



	Triode region	Saturation region
when	$\begin{cases} v_{GS} > V_{th} \\ v_{GS} - v_{DS} > V_{th} \end{cases}$	$\begin{cases} v_{GS} > V_{th} \\ v_{GS} - v_{DS} < V_{th} \end{cases}$
i_D	$k_n \left[(v_{GS} - V_{th}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$	$i_D = \frac{1}{2} k_n (v_{GS} - V_{th})^2$
i_S	$i_S = i_D$	$i_S = i_D$

QUESTION: Find out the resistance of R_D and R_S to bias the transistor at $I_D=0.4mA$ and $V_D=0.5V$ with $V_{th}=0.7V$, $V_{dd}=2.5V$, $V_{SS}=-2.5V$, $W=32\mu m$, $L=1\mu m$, $\mu_n C_{ox}=100\mu A/V^2$. Neglect the channel-length modulation effect.



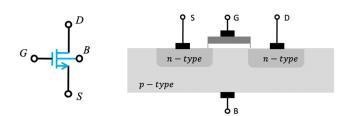
- Since $V_D = 0.5V$, $V_G = 0V$ $v_{GS} - v_{DS} = -0.5V < V_{th}$
- Assume the transistor is biased in saturation region
- According to KVL & transistor characteristics

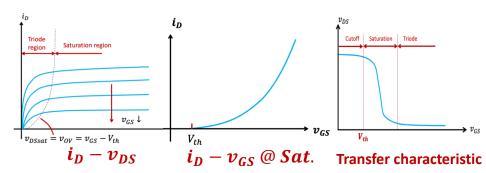
$$\begin{cases} V_{D} = V_{dd} - i_{D}R_{D} \\ V_{SS} + i_{D}R_{S} + V_{GS} = 0 \\ i_{D} = \frac{1}{2}k_{n}(v_{GS} - V_{th})^{2} \end{cases} \qquad \begin{cases} R_{D} = 5k\Omega \\ R_{S} = 3.25k\Omega \\ V_{GS} = 1.2V \end{cases}$$

Check assumption

Outline

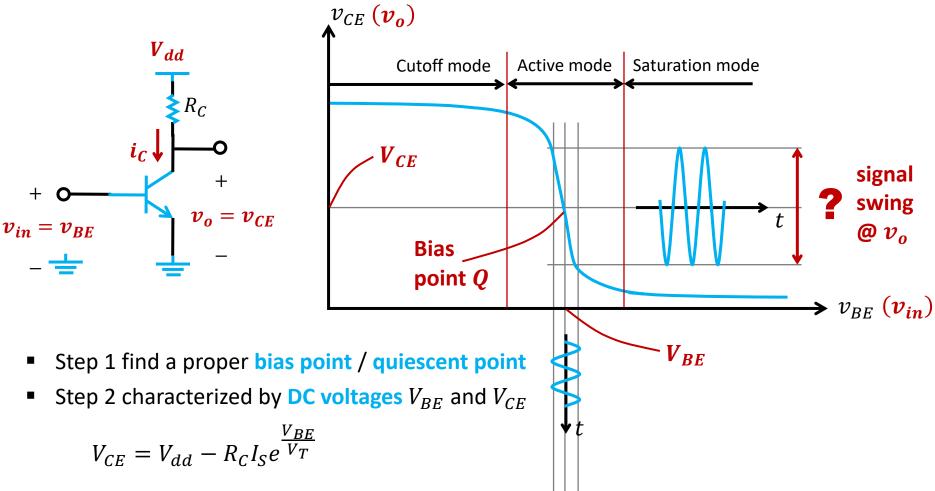
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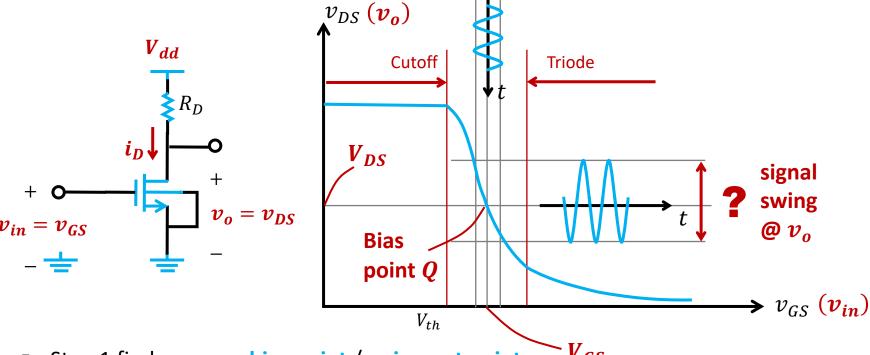
- Circuit analysis techniques with MOSFET
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 - AC analysis techniques

Recall: Signal Amplification of BJT



• Step 3 a sufficiently small voltage v_{BE} superimposed on V_{BE}

Signal Amplification of MOSFET

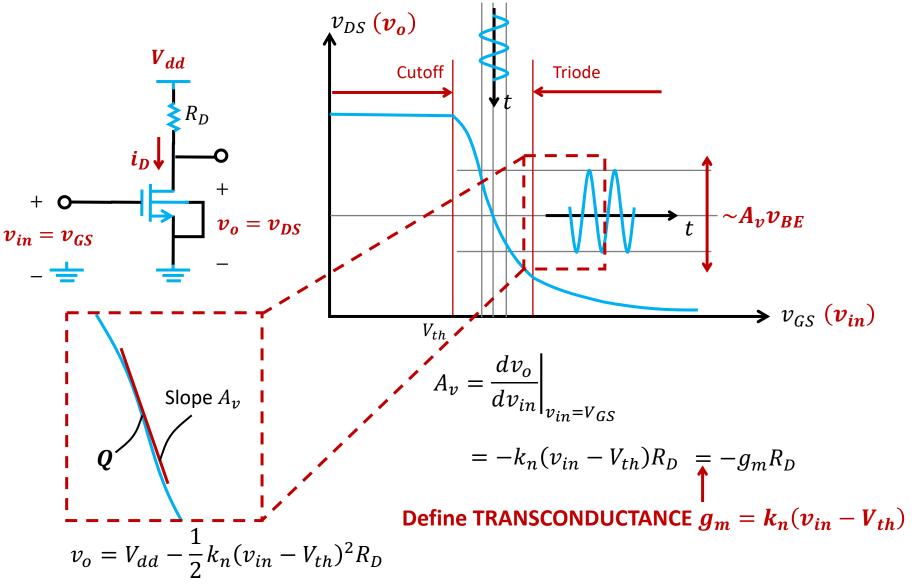


- Step 1 find a proper bias point / quiescent point
- Step 2 characterized by DC voltages V_{GS} and V_{DS}

$$V_{DS} = V_{dd} - R_D I_D = V_{dd} - \frac{1}{2} k_n (v_{GS} - V_{th})^2 R_D$$

Step 3 a sufficiently small voltage v_{GS} superimposed on V_{GS}

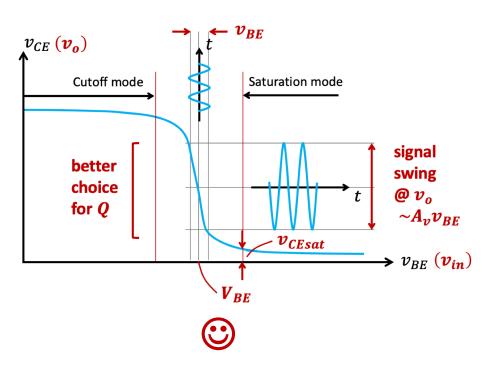
Signal Amplification of MOSFET

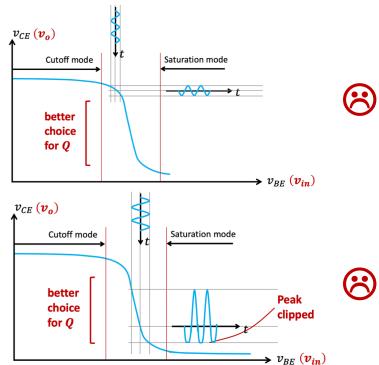


Recall: Locate the Bias Point for BJT

WHY? Key to small signal amplification

- Q is determined by V_{BE}
- Q determines the **GAIN** A_v
- Q has effects on the OUTPUT SIGNAL SWING



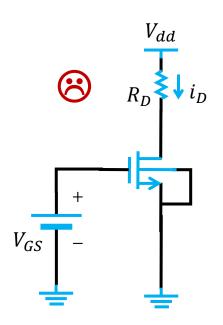


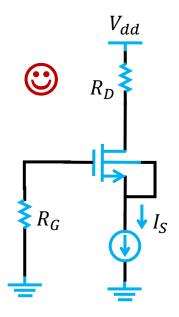
Locate the Bias Point for MOSFET

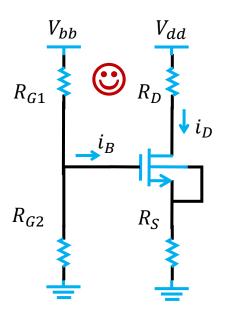
Method 1
By fixing V_{GS}

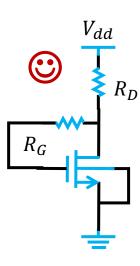
Method 2
By fixing I_S

- Method 3By fixing V_G &Connecting a R_S
- Method 4 –Using Drain-to-Gate feedback resistor



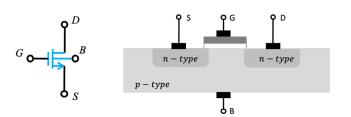


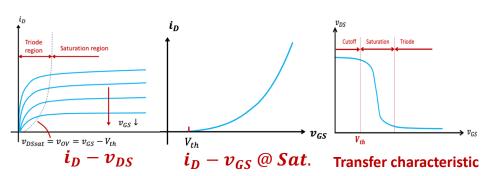




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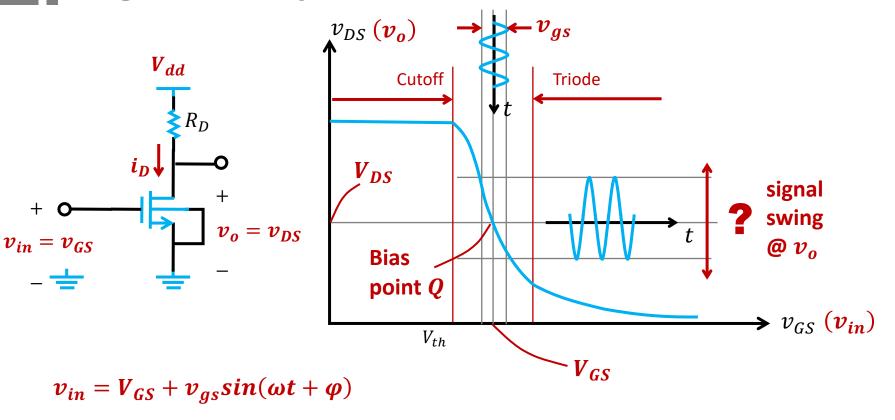
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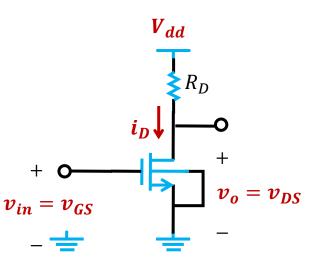
- Circuit analysis techniques with MOSFET
 - DC analysis techniques
 - AC analysis techniques
 - Locate the bias point
 - Small-signal operation & model

Signal Amplification of MOSFET



- The transistor is biased @ $v_{GS} = V_{GS}$
- A small AC signal is applied to input

Signal Amplification of MOSFET



Recall: Define

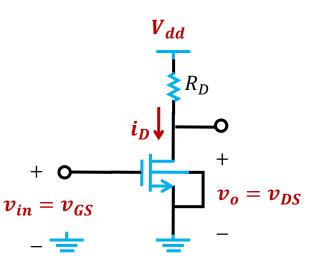
TRANSCONDUCTANCE $g_m = k_n(v_{in} - V_{th})$

$$v_{in} = V_{GS} + v_{gS}sin(\omega t + \varphi) = V_{GS} + v_{in,AC}$$

In saturation region, according to the transistor characteristic

$$\begin{split} i_D &= \frac{1}{2} k_n \big(V_{GS} + v_{in,AC} - V_{th} \big)^2 R_D \\ &= \frac{1}{2} k_n (V_{GS} - V_{th})^2 R_D + k_n (V_{GS} - V_{th}) v_{in,AC} + \frac{1}{2} k_n v_{in,AC}^2 R_D \\ &\downarrow I_D \\ &\approx I_D + \underbrace{k_n (V_{GS} - V_{th}) v_{in,AC}}_{C} \gg \frac{1}{2} v_{in,AC}^2 R_D \end{split}$$

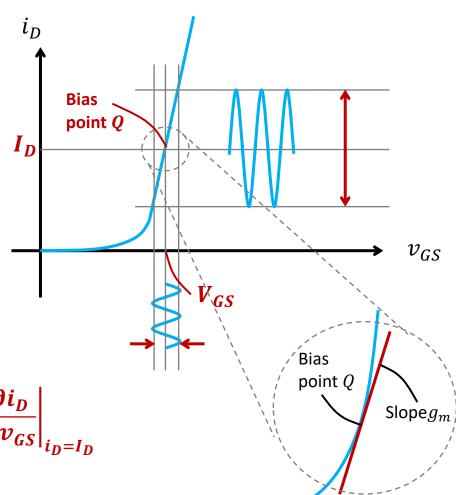
Transconductance g_m



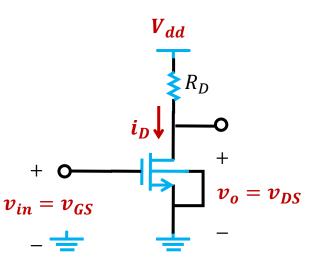
$$v_{in} = V_{GS} + v_{in,AC}$$

$$i_D = I_D + g_m v_{in,AC}$$

TRANSCONDUCTANCE
$$\left.g_{m}=rac{\partial i_{D}}{\partial v_{GS}}\right|_{i_{D}=I_{D}}$$



Voltage Gain A_{v}



$$v_{in} = V_{GS} + v_{in,AC}$$

$$i_D = I_D + g_m v_{in,AC}$$

$$g_m = \frac{\partial i_D}{\partial v_{GS}} \bigg|_{i_D = I_D}$$

According to KVL

$$v_{o} = V_{dd} - i_{D}R_{D} = V_{dd} - \left(i_{D}\Big|_{DC} + i_{D}\Big|_{AC}\right)R_{D}$$

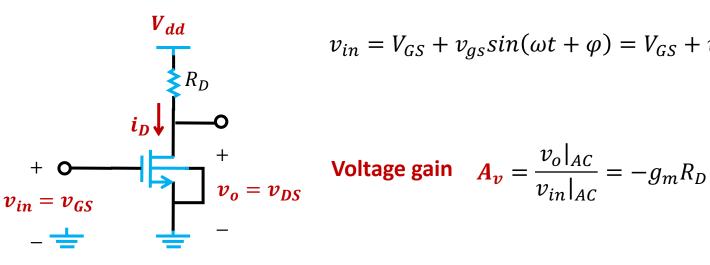
$$= V_{dd} - I_{D}R_{D} - i_{D}\Big|_{AC}R_{D}$$

$$V_{DS} = g_{m}v_{in,AC}$$

Define voltage gain

$$A_{v} = \frac{v_{o}|_{AC}}{v_{in}|_{AC}} = \frac{-g_{m}v_{in,AC}R_{D}}{v_{in,AC}} = -g_{m}R_{D}$$

Summary: Small-Signal Operation

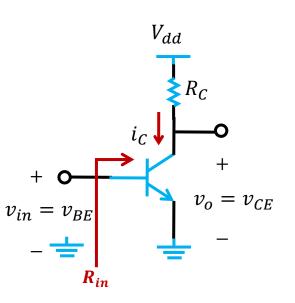


$$v_{in} = V_{GS} + v_{gS}sin(\omega t + \varphi) = V_{GS} + v_{in,AC}$$

Voltage gain
$$A_{oldsymbol{v}} = rac{v_o|_{AC}}{v_{in}|_{AC}} = -g_m R_D$$

Transconductance
$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{i_D = I_D} = k_n (V_{GS} - V_{th})$$

Recall: BJT Small-Signal Operation



$$v_{in} = V_{BE} + v_{be} sin(\omega t + \varphi) = V_{BE} + v_{AC}$$

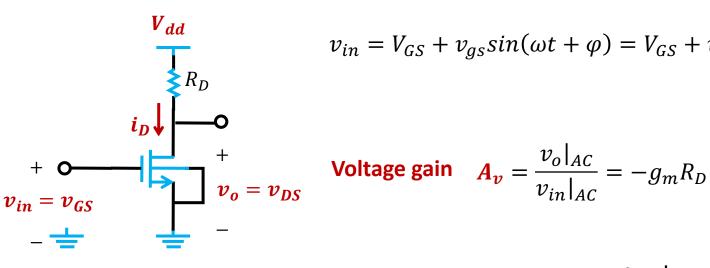
Voltage gain
$$A_v = \frac{v_o|_{AC}}{v_{in}|_{AC}} = -g_m R_C$$

Transconductance
$$g_m = \frac{\partial i_C}{\partial v_{BE}}\Big|_{i_C = I_C} = \frac{I_C}{V_T}$$

Input resistance @ Base
$$R_{in} = \frac{V_T}{I_B} = \frac{\beta}{g_m}$$

Why we don't discuss input resistance for MOSFET?

Summary: Small-Signal Operation

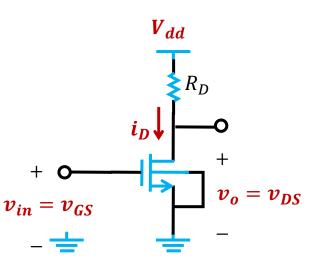


$$v_{in} = V_{GS} + v_{gS}sin(\omega t + \varphi) = V_{GS} + v_{in,AC}$$

Voltage gain
$$A_{oldsymbol{v}} = rac{v_o|_{AC}}{v_{in}|_{AC}} = -g_m R_L$$

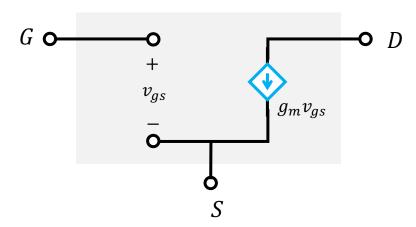
Transconductance
$$g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{i_D = I_D} = k_n (V_{GS} - V_{th})$$

Input resistance @ Base
$$R_{in} = \infty$$
 Since $i_G = 0$

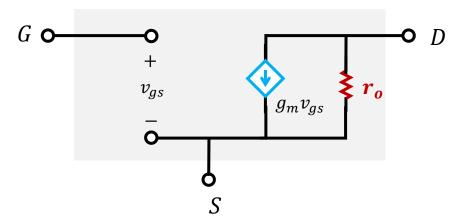


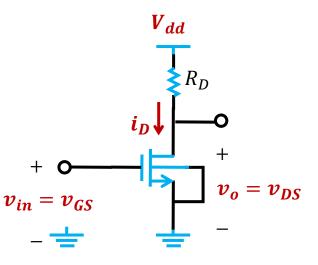
$$v_{in} = V_{GS} + v_{gS} sin(\omega t + \varphi) = V_{GS} + v_{in,AC}$$
 Voltage gain $A_v = \frac{v_o|_{AC}}{v_{in}|_{AC}} = -g_m R_D$ Transconductance $g_m = \frac{\partial i_D}{\partial v_{GS}}\Big|_{i_D = I_D} = k_n (V_{GS} - V_{th})$

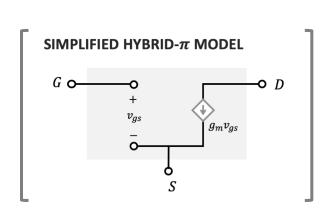
SIMPLIFIED HYBRID- π MODEL



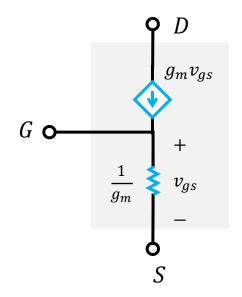
IF take channel-length modulation into account

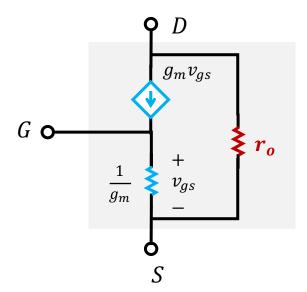






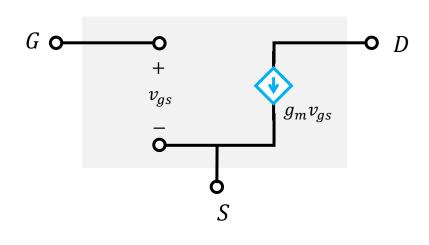
SIMPLIFIED T MODEL



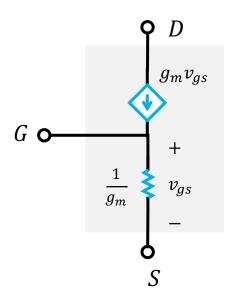


IF take channellength modulation into account

SIMPLIFIED HYBRID- π MODEL

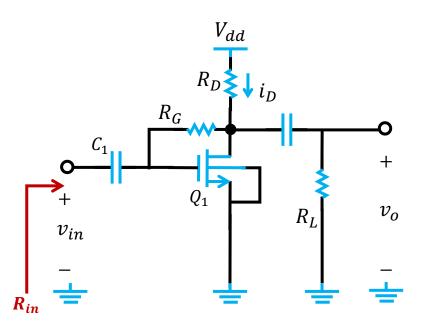


SIMPLIFIED T MODEL



HYBRID- π MODEL and T MODEL are equivalent

QUESTION: Find out the small-signal voltage gain A_v , input resistance R_{in} and the largest allowable input signal with $V_{th}=1.5V$, $V_{dd}=15V$, $V_A=50V$, $k_n=0.25\mu A/V^2$.

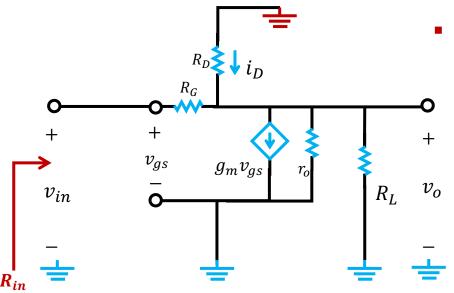


- Step 1: perform DC analysis
- Let's **ASSUME** Q_1 is biased in **Saturation mode**
- According to KVL & transistor characteristics

$$\begin{cases} v_{D} = V_{dd} - I_{D}R_{D} \\ I_{D} = \frac{1}{2}k_{n}(v_{GS} - V_{th})^{2} \end{cases} \begin{cases} I_{D} = 1.06mA \\ v_{D} = 4.4V \\ v_{GS} = v_{D} \end{cases}$$

Check assumption

QUESTION: Find out the small-signal voltage gain A_v , input resistance R_{in} and the largest allowable input signal with $V_{th}=1.5V$, $V_{dd}=15V$, $V_A=50V$, $k_n=0.25\mu A/V^2$.



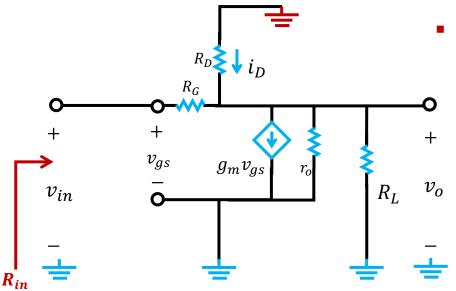
Step 2: perform AC analysis

- Step 2.1: replace the transistor with the small-signal model
- Step 2.2: turn off DC sources
 - SHORT all voltage sources
 - OPEN all current sources
- Step 2.3: Calculate small-signal model parameters

$$g_m = k_n(v_{GS} - V_{th}) = 0.725 mA/V$$

$$r_o = \frac{V_A}{I_D} = 47k\Omega$$

QUESTION: Find out the small-signal voltage gain A_v , input resistance R_{in} and the largest allowable input signal with $V_{th}=1.5V$, $V_{dd}=15V$, $V_A=50V$, $k_n=0.25\mu A/V^2$.



Step 2: perform AC analysis

Step 2.4: Analyze resulting circuit

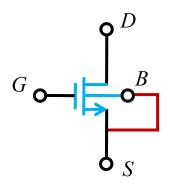
$$v_o = -g_m v_{gs}(R_D || R_L || r_o)$$
$$= -g_m v_{in}(R_D || R_L || r_o)$$

The voltage gain

$$A_{v} = \frac{v_{o}}{v_{in}} = -g_{m}(R_{D}||R_{L}||r_{o})$$

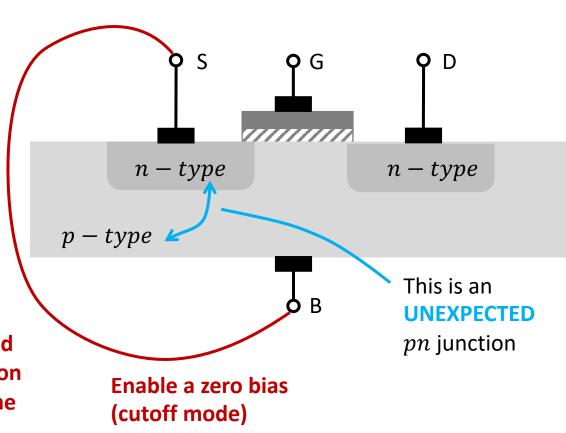
$$= -3.3$$

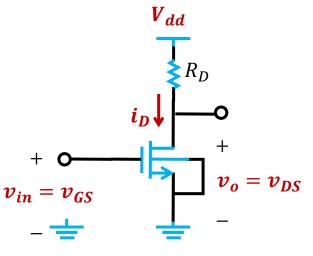
Recall: Body Effect of MOSFET



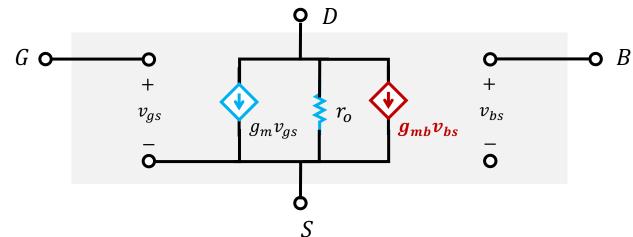
Enhancement-type NMOS transistor

BODY EFFECT: the substrate acts as a second gate when the pn junction between the base and the source is forward biased





IF take body effect into account

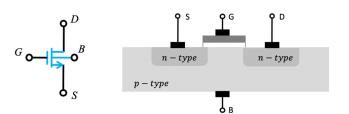


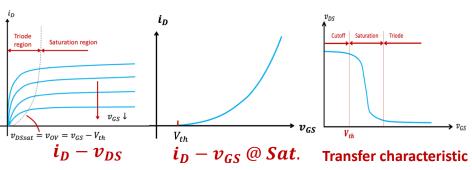
Define BODY TRANSCONDUCTANCE

$$\left.egin{aligned} g_{mb} = rac{\partial i_D}{\partial v_{BS}} \middle|_{\substack{v_{GS} = constant \ v_{DS} = constant}} \end{aligned} \end{aligned}$$

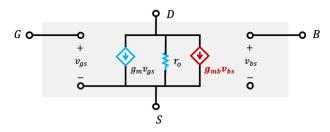
Outline

- Introduction to MOSFET
 - WHAT does it look like
 - HOW does it work
- The characteristic curves
 - $i_D v_{DS}$ characteristics
 - $varphi i_D v_{GS}$ characteristics
 - The transfer characteristic

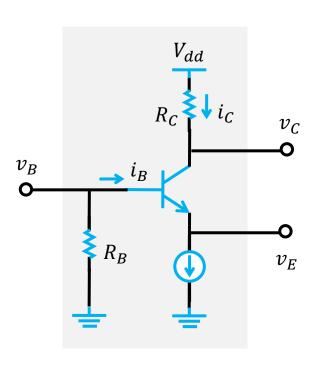




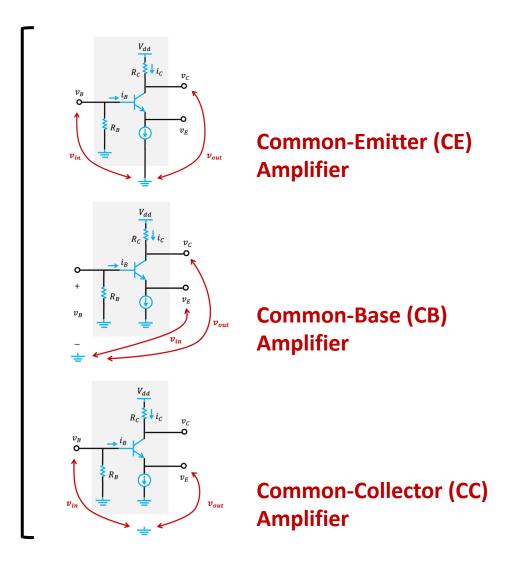
- Circuit analysis techniques with MOSFET
 - DC analysis techniques
 - AC analysis techniques
 - Locate the bias point
 - Small-signal operation & model
 - Basic BJT Amplifier Configurations



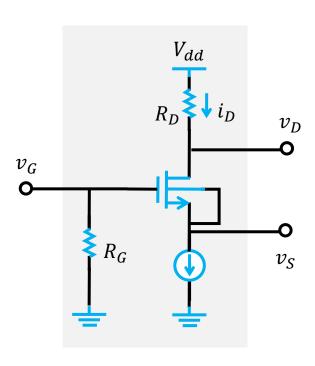
Recall: Basic BJT Amp. Configurations



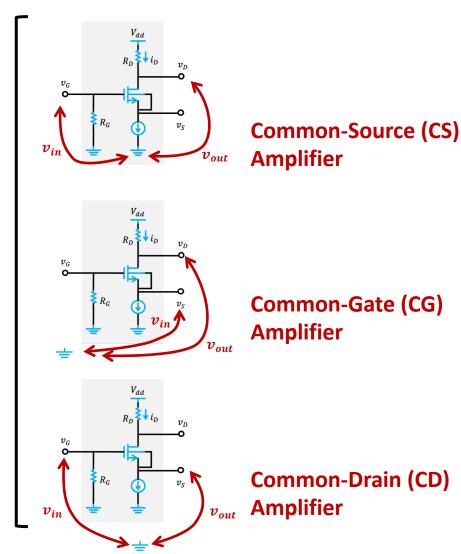
- Assume the transistor is biased in active mode
- There are three ports: Base,
 Collector and Emitter
- An amplifier requires two voltages: v_{in} and v_o



Basic MOSFET Amp. Configurations

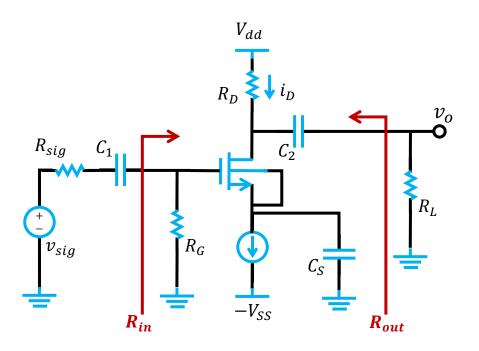


- Assume the transistor is biased in saturation mode
- There are three ports: Gate,
 Source and Drain
- An amplifier requires two voltages: v_{in} and v_o



Example 3: CS Amplifier

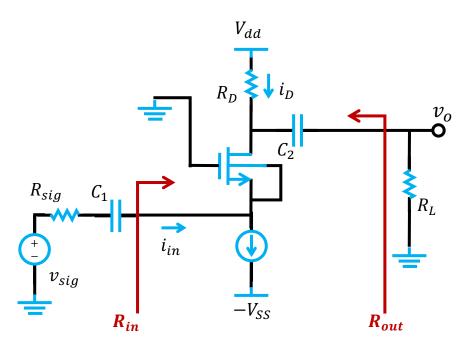
QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



- Step 1: perform DC analysis
- Step 2: perform AC analysis
 - Step 2.1: turn off DC sources
 - Step 2.2: Calculate small-signal model parameters, g_m
 - Step 2.3: replace the transistor with the small-signal model
 - Step 2.4: Analyze the resulting circuit

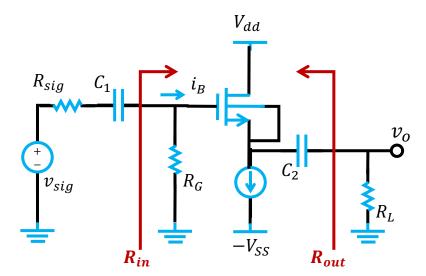
Example 4: CG Amplifier

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_D , C_1 , C_2 , V_{dd} , V_{SS} , and V_{th} . The body effect can not be neglected.



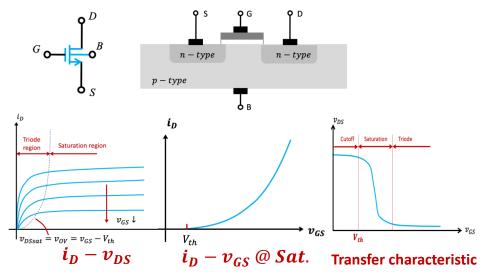
Example 5: CD Amplifier

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , C_1 , C_2 , V_{dd} , V_{SS} , and V_{th} .

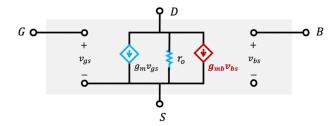


Outline

- Introduction to MOSFET
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 - $v_D v_{DS}$ characteristics
 - $v_D v_{GS}$ characteristics
 - The transfer characteristic

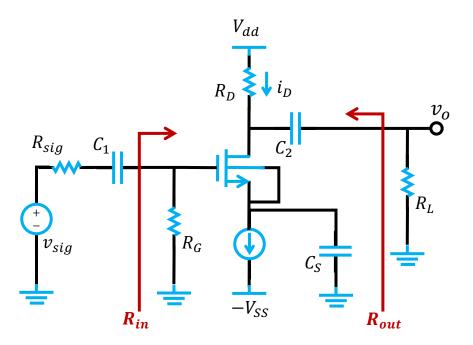


- Circuit analysis techniques with MOSFET
 - DC analysis techniques
 - AC analysis techniques
 - Locate the bias point
 - Small-signal operation & model
 - Basic BJT Amplifier Configurations
 - The frequency response



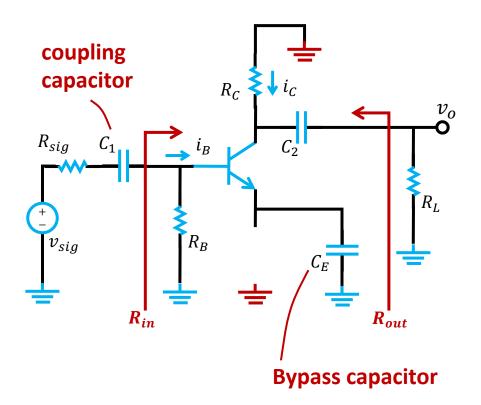
Example 6: CS Amp. w/ High Freq. Mod.

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



Recall: Example 5: CE Amplifier

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , R_B , R_C , C_1 , C_2 , C_E , V_{dd} , V_{SS} , and β .



Step 2: perform AC analysis

- Step 2.1: turn off DC sources
 - SHORT all voltage sources
 - OPEN all current sources

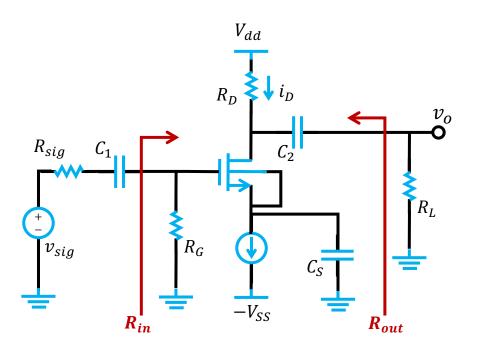
$$Z_{C_E} = \frac{1}{sC_E}$$

The bypass capacitor C_E provides a very LOW impedance to ground at all signal frequencies of interest

The coupling capacitor \mathcal{C}_1 and \mathcal{C}_2 act as perfect short circuit at all signal frequencies of interest

Example 6: CS Amp. w/ High Freq. Mod.

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .

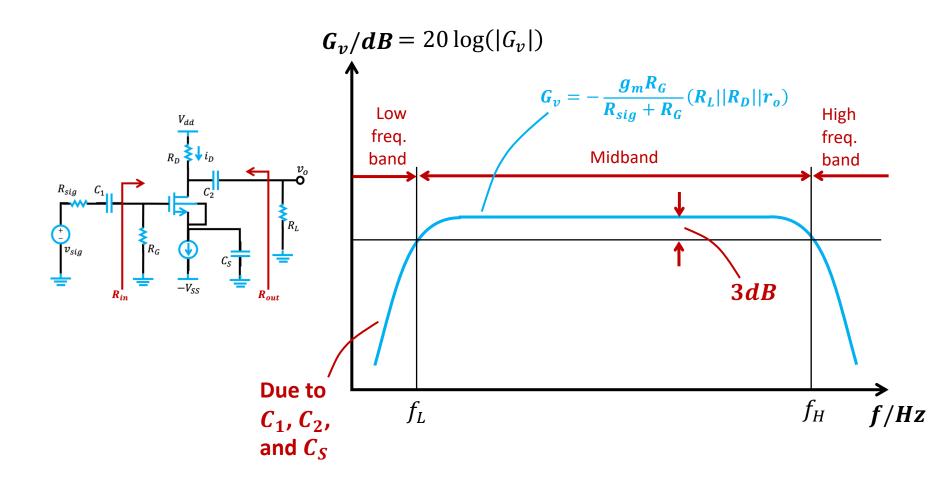


IDEALLY

- C_1 and C_2 are coupling capacitors
- C_S is bypass capacitor
- C_1 , C_2 , and C_S **IDEALLY** are short circuit @DC

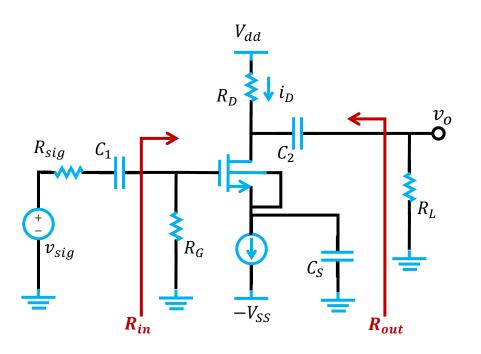
WHAT HAPPEN IN A REAL SCENARIO?

The Frequency Response



Example 6: CS Amp. w/ High Freq. Mod.

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



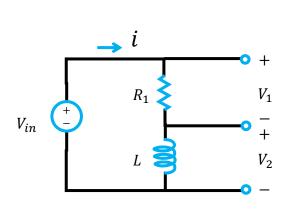
- Check the effect from C₁
- According to KVL

$$v_{G} = \frac{R_{G}}{R_{sig} + \frac{1}{sC_{1}} + R_{G}} v_{sig}$$

$$= v_{sig} \frac{R_{G}}{R_{sig} + R_{G}} \frac{1}{1 + \frac{1}{sC_{1}(R_{sig} + R_{G})}}$$

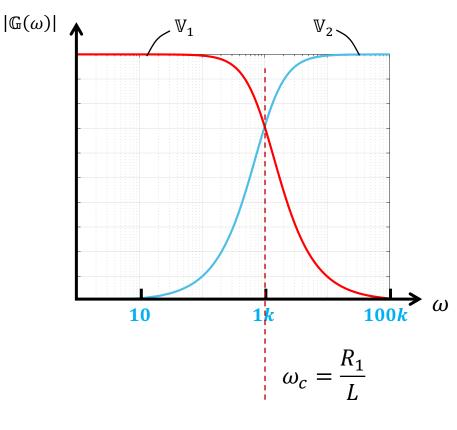
Recall: Transfer Function for HPF

QUESTION: design a stereo amplifier with two output channels to split the high and low frequencies.

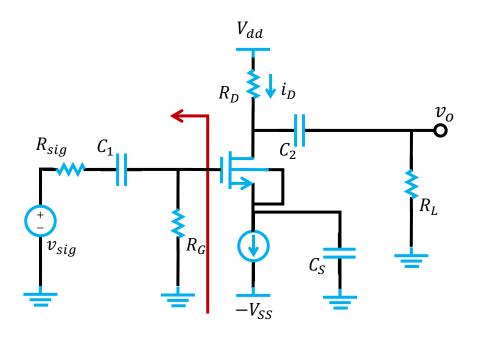


$$\mathbb{G}_{1}(\omega) = \frac{\mathbb{V}_{1}}{\mathbb{V}_{in}} = \frac{R_{1}}{R_{1} + j\omega L}$$

$$\mathbb{G}_{2}(\omega) = \frac{\mathbb{V}_{2}}{\mathbb{V}_{in}} = \frac{j\omega L}{R_{1} + j\omega L}$$



QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



- Check the effect from C_1
- According to KVL

$$v_G = \frac{R_G}{R_{sig} + \frac{1}{sC_1} + R_G} v_{sig}$$

$$= v_{sig} \frac{R_G}{R_{sig} + R_G} \frac{s}{s + \frac{1}{C_1(R_{sig} + R_G)}}$$

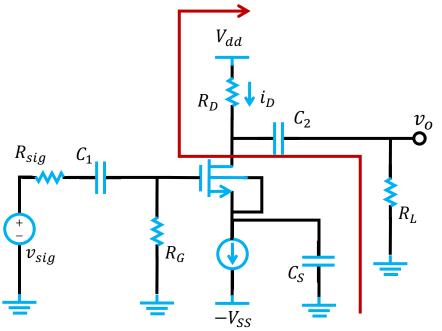
a Lliab D

This is a High Pass

$$\omega_{L1} = \frac{1}{C_1(R_{sig} + R_G)}$$

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} ,

 R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



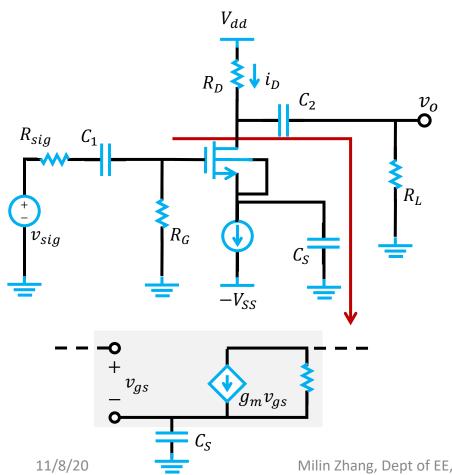
- Check the effect from C₂
- According to KVL

$$v_{out} = -i_d \frac{R_D R_L}{R_D + R_L + \frac{1}{sC_2}}$$
$$= -i_d R_L \frac{s}{s + \frac{1}{C_2(R_D + R_L)}}$$

This is a High Pass

$$\omega_{L2} = \frac{1}{C_2(R_D + R_L)}$$

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



- Check the effect from C_S
- According to KVL

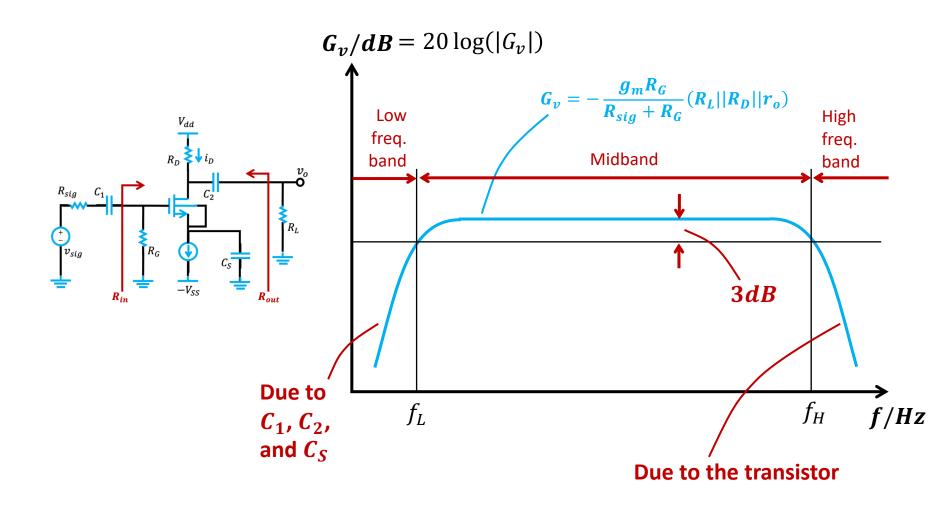
$$v_G - g_m v_{gs} \frac{1}{sC_S} = v_{gs}$$

$$v_{gs} = \frac{s}{s + \frac{g_m}{C_S}} v_G$$
This is a High Pa

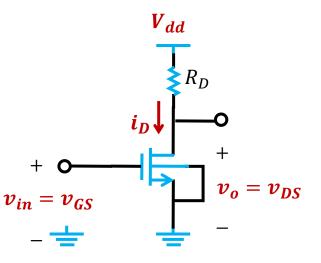
This is a High Pass

$$\omega_{L3} = \frac{g_m}{C_S}$$

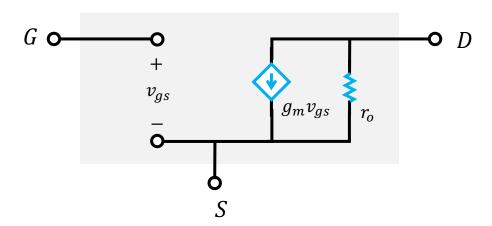
The Frequency Response



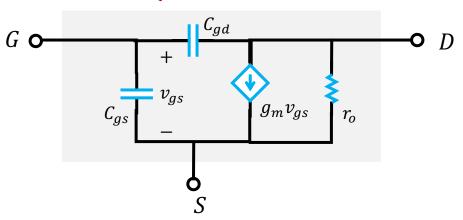
Small-Signal Model



SIMPLIFIED HYBRID- π MODEL

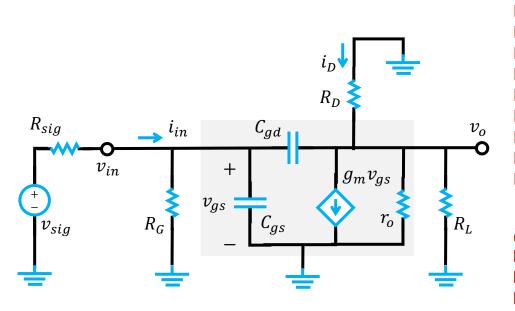


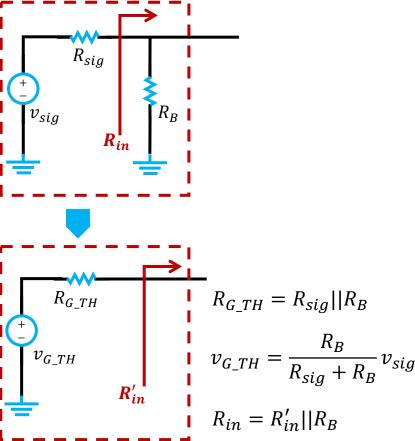
THE HIGH FREQUENCY MODEL



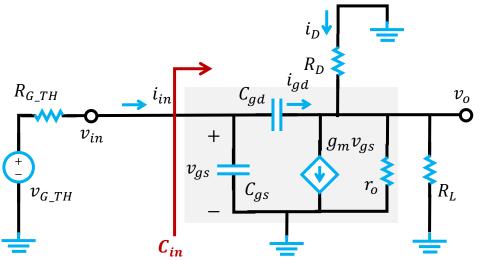
QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} ,

 R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .





QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



 According to KVL & KCL, and device characteristics

$$v_{out} = (-g_m v_{gs} + i_{gd})(R_L||R_D||r_o)$$

$$g_m v_{gs} \gg i_{gd}$$

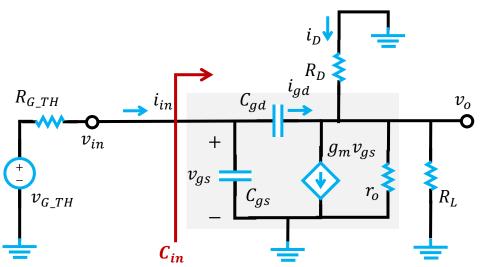
$$\approx -g_m v_{gs} R'_L$$

$$i_{gd} = (v_{gs} - v_{out})sC_{gd}$$

$$= (1 + g_m R'_L)sC_{gd}v_{gs}$$

$$i_{in} = i_{gs} + i_{gd} = (C_{gs} + C_{gd}(1 + g_m R'_L))sv_{gs}$$
Define C_{in}

QUESTION: Find out the voltage gain, the input and output resistances with given v_{in} , R_{sig} , k_n , R_G , R_D , C_1 , C_2 , C_S , V_{dd} , V_{SS} , and V_{th} .



$$R_{G_TH} = R_{sig} || R_B$$

$$v_{G_TH} = \frac{R_B}{R_{sig} + R_B} v_{sig}$$

$$C_{in} = C_{gs} + C_{gd} (1 + g_m R'_L)$$

The overall gain

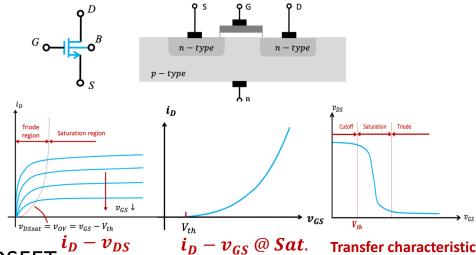
$$G_{v} = \frac{v_{o}}{v_{sig}} = \frac{-g_{m}v_{gs}R'_{L}}{v_{sig}}$$

$$= \frac{-g_{m}R'_{L}}{v_{sig}} \frac{v_{G_TH}}{1 + sR_{G_TH}C_{in}}$$

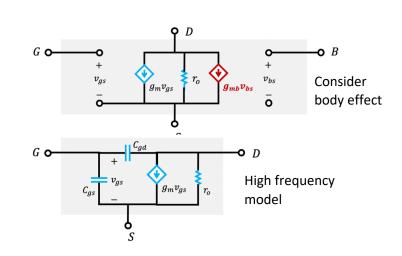
$$= \begin{bmatrix} -\frac{g_{m}R'_{L}R_{G}}{R_{sig} + R_{G}} \end{bmatrix} \frac{1}{1 + sR_{G_TH}C_{in}}$$
Midband
$$Gain \qquad \omega_{H1} = \frac{1}{R_{G_TH}C_{in}}$$

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- Circuit analysis techniques with MOSFET
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MOSFET v.s. BJT

	NMOS	npn BJT
Circuit symbol		B O E
Physical Structure	n - type $p - type$ B	O C O B O E n p

MOSFET v.s. BJT

	NMOS	npn BJT
To Operate in Active mode	biased in saturation region $v_{GS} > V_{th}$	biased in active region $V_{BE} > V_{BEon}$ L EBJ forward biased $V_{BC} < V_{BCon}$ L CBJ reverse biased
Characteristics in active mode	$i_D = (\mu_n C_{ox}) \left(\frac{W}{L}\right) \left[(v_{GS} - V_{th}) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$ $i_G = 0$	$i_C = I_S e^{rac{v_{BE}}{V_T}} \left(1 + rac{v_{CE}}{V_A} ight)$ $i_B = i_C/eta$

MOSFET v.s. BJT

	NMOS	npn BJT
The small signal model	$G \circ O \circ D \circ D$	$r_{\pi} = \frac{\beta}{g_m}$ $r_{\pi} = \frac{\beta}{g_m}$ E
High frequency model	$G \circ \bigcup_{c_{gs}} C_{gd} \circ D$ $C_{gs} \bigcup_{c_{gs}} C_{ggs} \circ D$ S	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$
Transconductance	$\mathbf{g_m} = k_n (V_{GS} - V_{th})$	$g_m = \frac{I_C}{V_T}$
Input resistance w/ Source/Emitter grounded	$R_{in} = \infty$	$R_{in} = \frac{V_T}{I_B} = \frac{\beta}{g_m}$

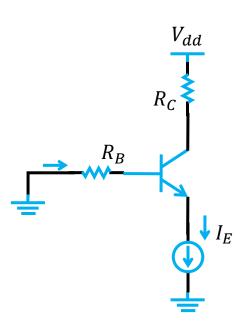
Outline

- Introduction to MOSFET
- The characteristic curves
- Circuit analysis techniques with MOSFET
 - DC analysis techniques
 - AC analysis techniques
 - The frequency response
- MOSFET v.s. BJT
- More examples of useful modules
 - Current sources

Recall: HOW to Locate the Bias Point

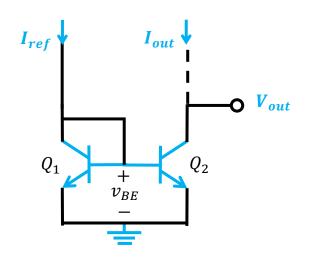
Method 3 – Using Constant-Current Source





- I_E is independent of β and R_B
- How to realize a current source?
 - Current mirror explained in next chapter

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- Since Q_1 and Q_2 are matched $\beta_{Q_1} = \beta_{Q_2} = \beta$
- According to the BJT characteristic

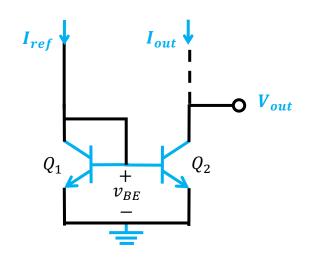
$$I_{C1} = I_S e^{\frac{v_{BE1}}{V_T}}$$
 and $I_{out} = I_{C2} = I_S e^{\frac{v_{BE2}}{V_T}}$

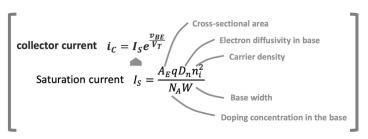
According to KCL

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta}$$

$$\frac{I_{out}}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta}} \xrightarrow{\beta \to \infty} 1$$

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.





• What if the area of EBJ of Q_2 is m times of Q_1 ?

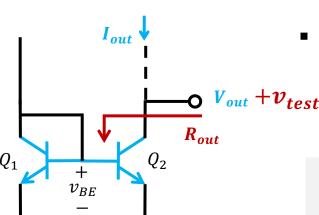
$$I_{S2} = mI_{S1}$$

According to the BJT characteristic

$$I_{C1} = I_{S1}e^{\frac{v_{BE1}}{V_T}}$$
 and $I_{out} = I_{C2} = I_{S2}e^{\frac{v_{BE2}}{V_T}}$

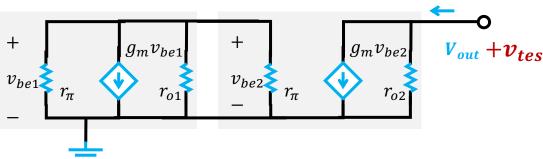
$$\frac{I_{out}}{I_{ref}} = \frac{m}{1 + \frac{1}{\beta} + \frac{m}{\beta}} \xrightarrow{\beta \to \infty} m$$

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- Step 1: remove I_{ref}
- Step 2: Apply a SMALL testing voltage. Look for ΔI_{out}

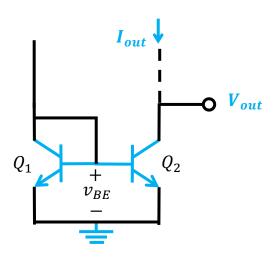




 $R_o = \infty$ if neglect the Early Effect Ideal current source

Iout

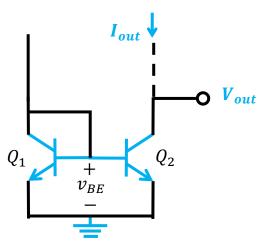
QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- If take the Early Effect into account
- According to the BJT characteristic

$$\begin{split} I_{C1} &= I_S e^{\frac{v_{BE1}}{V_T}} \left(1 + \frac{V_{CE1}}{V_{A1}} \right) \\ I_{out} &= I_{C2} = mI_S e^{\frac{v_{BE2}}{V_T}} \left(1 + \frac{V_{CE2}}{V_{A2}} \right) \\ I_{B1} &\approx \frac{1}{\beta} I_S e^{\frac{v_{BE1}}{V_T}} \\ I_{B2} &\approx \frac{1}{\beta} I_S e^{\frac{v_{BE2}}{V_T}} \end{split}$$

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



According to KCL

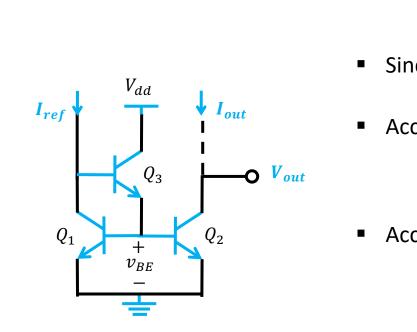
$$I_{ref} = I_{C1} + I_{B1} + I_{B2} = \frac{m\left(1 + \frac{V_{CE2}}{V_{A2}}\right)}{\left(1 + \frac{V_{CE1}}{V_{A1}}\right) + \frac{1+m}{\beta}}$$

$$\approx \frac{m\left(1 + \frac{V_{CE2}}{V_{A2}}\right)}{\left(1 + \frac{V_{CE1}}{V_{A1}}\right) + \frac{1+m}{\beta}\left(1 + \frac{V_{CE1}}{V_{A1}}\right)} = \frac{m}{1 + \frac{1+m}{\beta}}\left(1 + \frac{V_{CE2}}{V_{A2}}\right)$$

$$\approx \frac{m}{1 + \frac{1+m}{\beta}}\left(1 + \frac{V_{CE2}}{V_{A2}}\right)\left(1 - \frac{V_{CE1}}{V_{A1}}\right) \approx \frac{m}{1 + \frac{1+m}{\beta}}\left(1 + \frac{V_{CE2}}{V_{A2}} - \frac{V_{CE1}}{V_{A1}}\right)$$

$$= \frac{m}{1 + \frac{1+m}{\beta}}\left(1 + \frac{V_{out} - V_{BE}}{V_{A2}}\right)$$
The error term $\frac{V_{out} = V_{BE}}{V_{Out} = V_{BE}}$

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- Since Q_1 and Q_2 are matched $\beta_{Q_1} = \beta_{Q_2} = \beta$
- According to the BJT characteristic

$$I_{C1} = I_S e^{\frac{v_{BE1}}{V_T}}$$
 and $I_{out} = I_{C2} = I_S e^{\frac{v_{BE2}}{V_T}}$

According to KCL

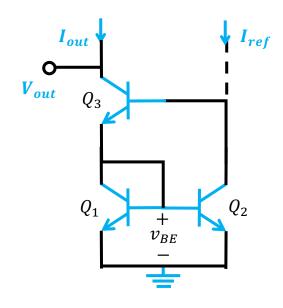
$$I_{ref} = I_{C1} + I_{B3} = I_{C1} + \frac{I_{E3}}{1 + \beta}$$

$$\frac{I_{out}}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta^2 + \beta}} \xrightarrow{\beta \to \infty} \frac{1}{1 + \frac{2}{\beta^2}}$$

• The output resistance $R_o = r_{o2} = \frac{V_{A2}}{I_{out}}$

Example 8: Wilson current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- Since Q_1 and Q_2 are matched $\beta_{Q_1} = \beta_{Q_2} = \beta$
- According to the BJT characteristic

$$I_{C1} = I_{C2} = I_S e^{\frac{v_{BE}}{V_T}}$$
 and $I_{out} = I_{C3} = \frac{\beta}{1 + \beta} I_{E3}$

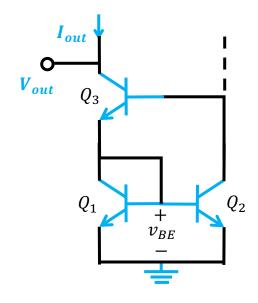
According to KCL

$$\begin{cases} I_{ref} = I_{C2} + I_{B3} = \frac{1 + 2/\beta}{1 + \beta} I_{C1} + I_{C2} \\ I_{out} = \frac{\beta}{1 + \beta} (I_{C1} + I_{B1} + I_{B2}) \end{cases}$$

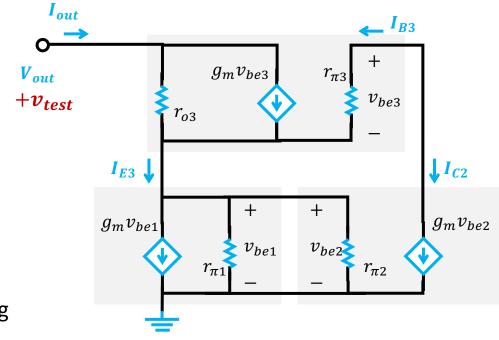
$$\frac{I_{out}}{I_{ref}} = \frac{1}{1 + \frac{2}{\beta(\beta + 2)}} \xrightarrow{\beta \to \infty} \frac{1}{1 + \frac{2}{\beta^2}}$$

Example 8: Wilson current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.

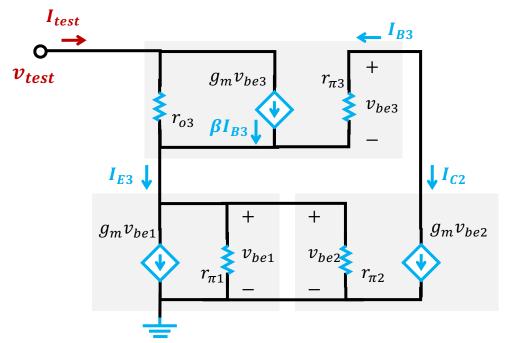


- Step 1: remove I_{ref}
- Step 2: Apply a **SMALL** testing voltage. Look for ΔI_{out}



Example 8: Wilson current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



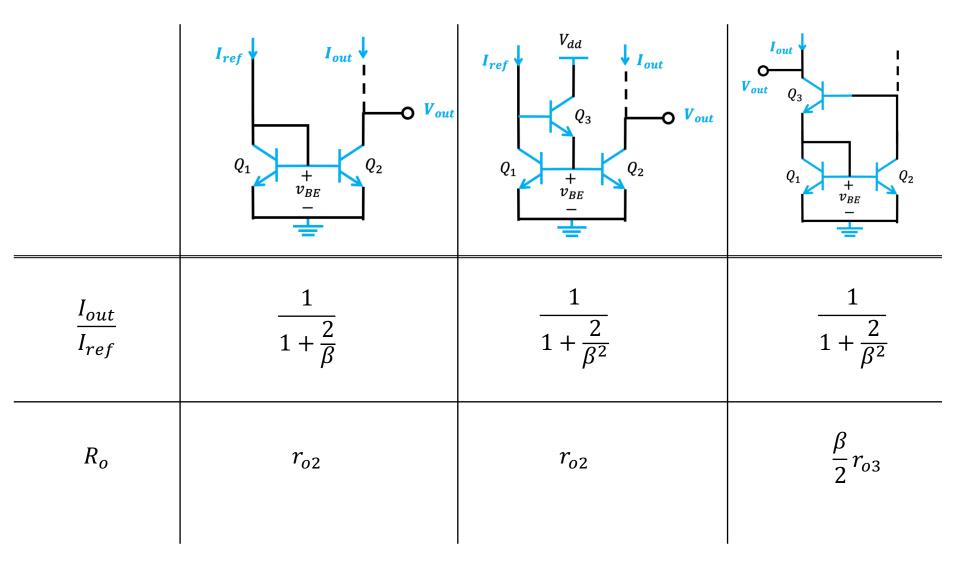
According to KCL

$$\begin{cases} I_{E3} = \frac{I_{C1}}{\beta} + \frac{I_{C2}}{\beta} + I_{C1} \\ I_{E3} = I_{r_{o3}} + \beta I_{B3} + I_{B3} \\ I_{C1} = I_{C2} = -I_{B3} \end{cases}$$

The input resistance

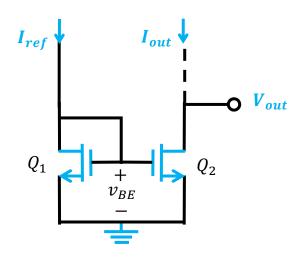
$$R_{o} = \frac{v_{test}}{I_{test}} = \frac{r_{o3} I_{r_{o3}}}{I_{r_{o3}} + \beta I_{B3}} = \frac{\left(\frac{2}{\beta} + 2 + \beta\right) I_{C1} r_{o3} + \frac{1}{\beta} I_{C1} r_{\pi 1}}{\left(\frac{2}{\beta} + 1\right) I_{C1}} \approx \frac{\beta}{2} r_{o3}$$

Summary: BJT current mirror



Example 9: MOSFET current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



- Since Q_1 and Q_2 are matched $k_{n,Q_1} = k_{n,Q_2} = k_n$
- According to the MOSFET characteristic

$$\begin{cases} v_{GS} > V_{th} \\ v_{GS} - v_{DS} = 0 < V_{th} \end{cases}$$

Saturation region

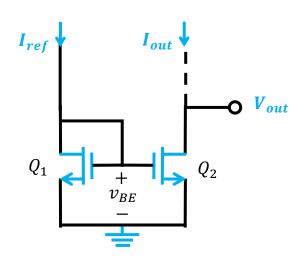
$$I_{ref} = \frac{1}{2} k_{n,Q_1} (V_{GS1} - V_{th})^2$$

$$I_{out} = \frac{1}{2} k_{n,Q_2} (V_{GS1} - V_{th})^2$$

$$\frac{I_{out}}{I_{ref}} = 1$$

Example 9: MOSFET current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



• What if
$$\left(\frac{W}{L}\right)_2 \neq \left(\frac{W}{L}\right)_1$$

According to the MOSFET characteristic

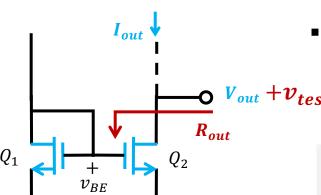
$$I_{ref} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_1 (V_{GS1} - V_{th})^2$$

$$I_{out} = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L} \right)_2 (V_{GS1} - V_{th})^2$$

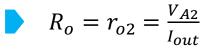
$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1}$$

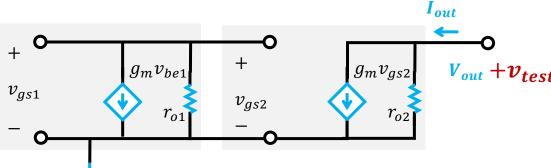
Example 9: MOSFET current mirror

QUESTION: Find out the relationship between I_{ref} and I_{out} with Q_1 and Q_2 are matched.



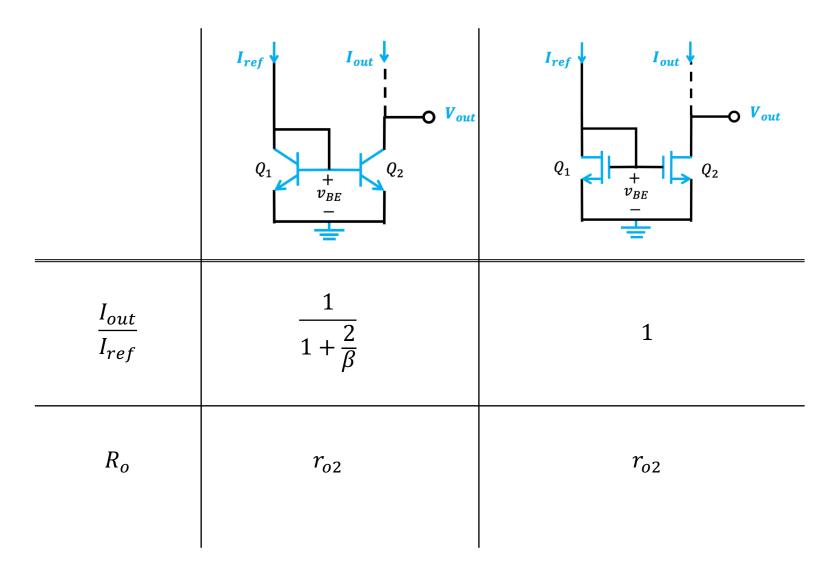
- Step 1: remove I_{ref}
- Step 2: Apply a SMALL testing voltage. Look for ΔI_{out}





 $R_o = \infty$ if neglect the Early Effect

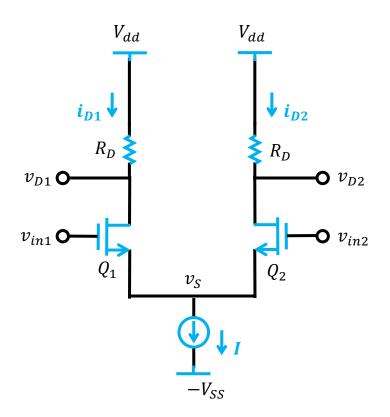
MOSFET v.s. BJT current mirror



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 - The MOS differential pair

What is MOS Differential Pair



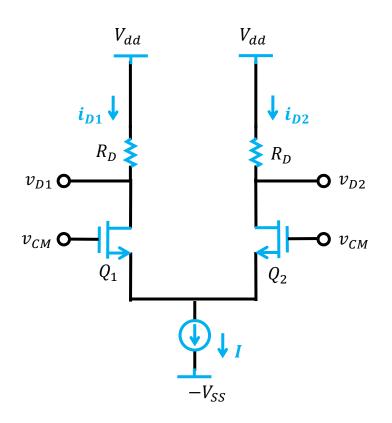
Features of MOS differential pair

Two matched transistors

$$\left(\mu_n C_{ox} \frac{W}{L}\right)_1 = \left(\mu_n C_{ox} \frac{W}{L}\right)_2 = \mu_n C_{ox} \frac{W}{L}$$

- The two Sources are joined together
- A constant current source for biasing connected to the sources
- The transistors are typically biased in saturation region

Operation w/ Common-Mode Input



According to KCL

$$i_{D1} = i_{D2} = \frac{1}{2}I$$

Assume the trans. are biased in sat. region

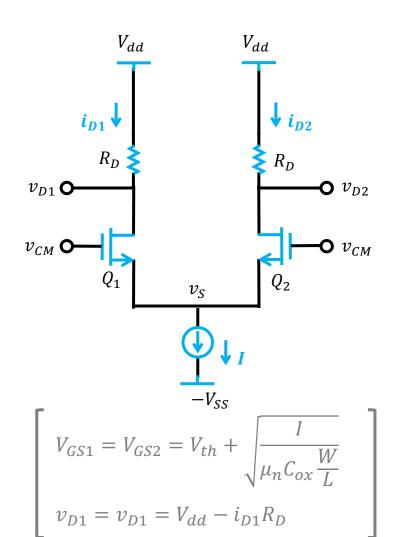
$$\begin{cases} i_{D1} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{th})^2 \\ i_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS2} - V_{th})^2 \end{cases}$$

$$V_{GS1} = V_{GS2} = V_{th} + \sqrt{\frac{I}{\mu_n C_{ox} \frac{W}{L}}}$$

According to KVL

$$v_{D1} = v_{D1} = V_{dd} - i_{D1}R_{D}$$

Operation w/ Common-Mode Input



$$\begin{tabular}{ll} \blacksquare & \begin{tabular}{ll} \end{tabular} \begin{tabular}{ll} $v_{GS} > V_{th}$ & to fit the \\ $v_{GD} < V_{th}$ & assumption \\ \end{tabular}$$

• The highest value of v_{CM}

$$v_{CM,max} = V_{dd} - i_{D1}R_D + V_{th}$$

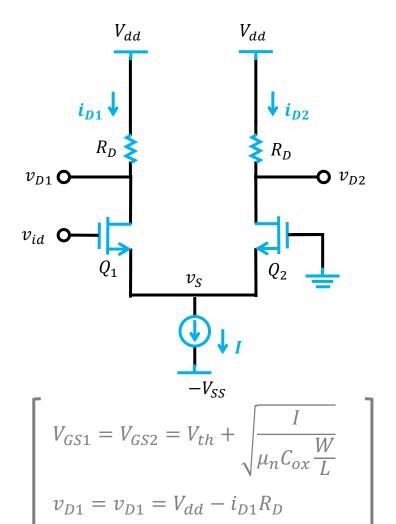
• The lowest value of v_{CM}

$$v_{CM,min} = -V_{SS} + V_{CurSrc} + V_{GS}$$

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Operation w/ Differential-Mode Input



According to KVL

$$v_{id} - v_{GS1} = v_{in2} - v_{GS2}$$

- $v_{id} = v_{GS1} v_{GS2}$
- Define differential output $v_{od} = v_{D2} v_{D1}$
- Assume the trans. are biased in sat. region

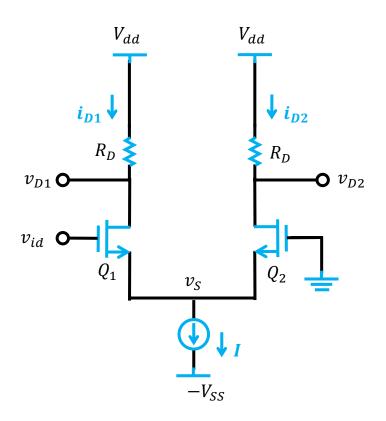
$$i_{D1} > i_{D2}$$
 if $v_{id} > 0$

$$v_{od} = v_{D2} - v_{D1} > 0$$

$$i_{D1} < i_{D2}$$
 if $v_{id} < 0$

$$v_{od} = v_{D2} - v_{D1} < 0$$

Operation w/ Differential-Mode Input



- Let's find the range of v_{id}
- lacktriangle A highest value of v_{id} is achieved when

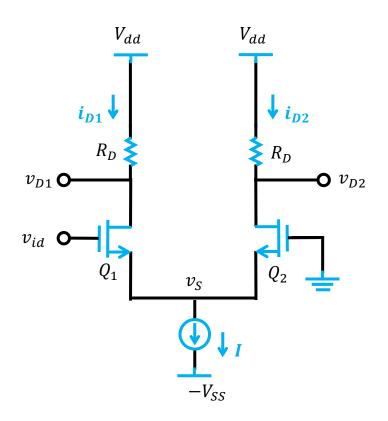
$$\begin{cases} i_{D1} = I \\ i_{D2} = 0 \quad with \ v_{GS2} = V_{th} \end{cases}$$

- $v_{GS1} = v_{id,max} + V_{th}$
- Assume the trans. are biased in sat. region

$$I = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS1} - V_{th})^2$$

$$v_{id,max} = \sqrt{\frac{2I}{k_n}}$$

Operation w/ Differential-Mode Input



- Let's find the range of v_{id}
- Similarly, the lowest value of v_{id} is

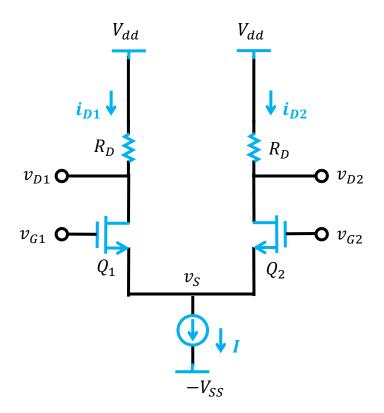
$$v_{id,min} = -\sqrt{\frac{2I}{k_n}}$$

NOTE: both of the transistors are biased in the saturation region

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 - Large-signal operation

Large-Signal Operation



DEFINE **DIFFERENTIAL INPUT** $v_{id} = v_{G1} - v_{G2}$

ASSUME $Q_1 \& Q_2$ are biased in saturation region

According to characteristic

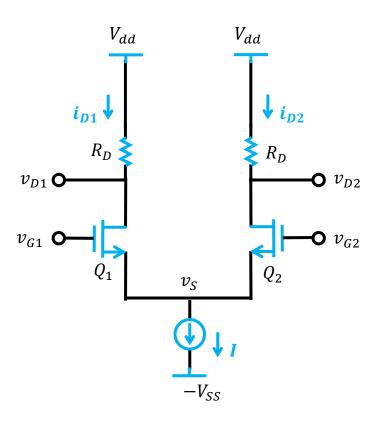
$$\begin{cases} i_{D1} = \frac{1}{2} k_n (V_{GS1} - V_{th})^2 \\ i_{D2} = \frac{1}{2} k_n (V_{GS2} - V_{th})^2 \end{cases}$$

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}} k_n (v_{GS1} - v_{GS2})$$

According to KCL

$$i_{D1} + i_{D2} = I$$

Large-Signal Operation



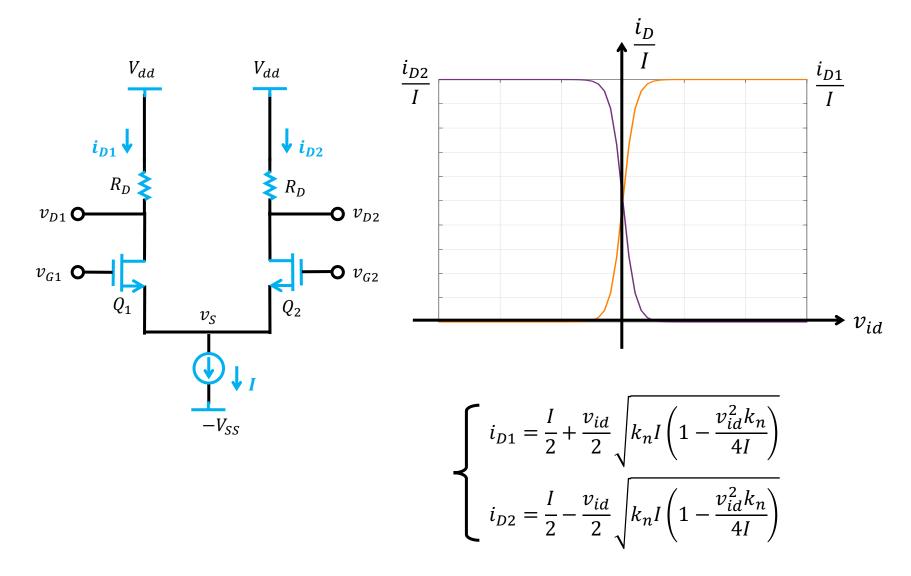
$$\begin{cases} \sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{\frac{1}{2}} k_n (v_{GS1} - v_{GS2}) \\ i_{D1} + i_{D2} = I \end{cases}$$

$$\begin{cases} i_{D1} = \frac{I}{2} + \frac{v_{id}}{2} \sqrt{k_n I \left(1 - \frac{v_{id}^2 k_n}{4I}\right)} \\ i_{D2} = \frac{I}{2} - \frac{v_{id}}{2} \sqrt{k_n I \left(1 - \frac{v_{id}^2 k_n}{4I}\right)} \end{cases}$$

• If
$$v_{id} = 0$$

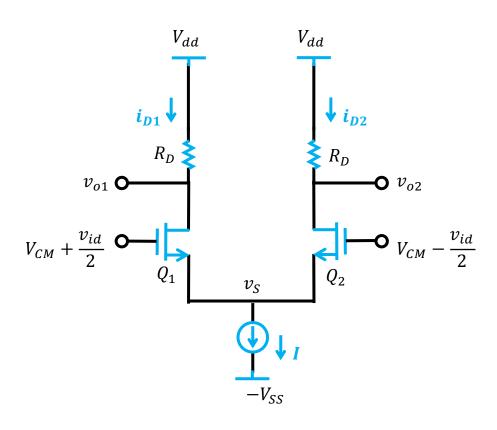
If
$$v_{id} = 0$$
 $i_{D1} = i_{D2} = \frac{I}{2}$

Large-Signal Operation



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 - Operation w/ differential-mode input
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 - Small-signal operation

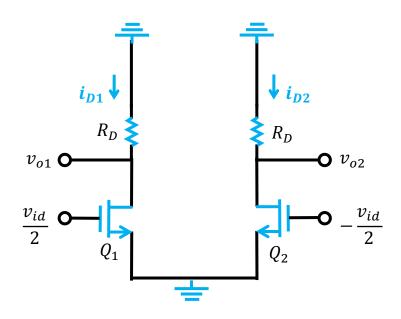


 V_{CM} is a DC input

 $\frac{v_{id}}{2}$ is a very small AC signal

Step 1: perform DC analysis

$$I_{D1} = I_{D2} = \frac{I}{2}$$



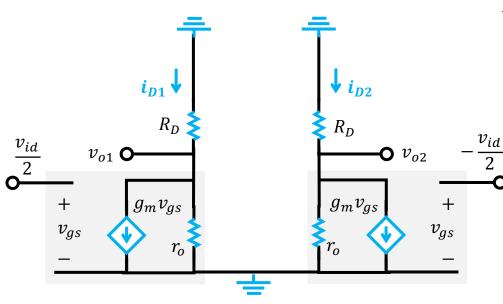
 V_{CM} is a DC input

 $\frac{v_{id}}{2}$ is a very small AC signal

Step 1: perform DC analysis

$$I_{D1} = I_{D2} = \frac{I}{2}$$

- Step 2: perform AC analysis
 - Step 2.1: turn off DC sources
 - □ Step 2.2: Calculate small-signal model parameters, g_m



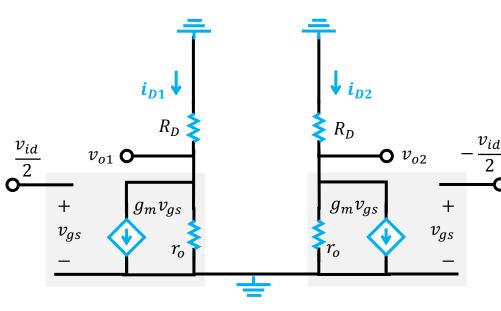
 V_{CM} is a DC input

 $\frac{v_{id}}{2}$ is a very small AC signal

Step 1: perform DC analysis

$$I_{D1} = I_{D2} = \frac{I}{2}$$

- Step 2: perform AC analysis
 - Step 2.1: turn off DC sources
 - Step 2.2: Calculate small-signal model parameters, g_m
 - Step 2.3: replace the transistor with the small-signal model
 - Step 2.4: Analyze the resulting circuit



 V_{CM} is a DC input

 $\frac{v_{id}}{2}$ is a very small AC signal

Step 1: perform DC analysis

$$I_{D1} = I_{D2} = \frac{I}{2}$$

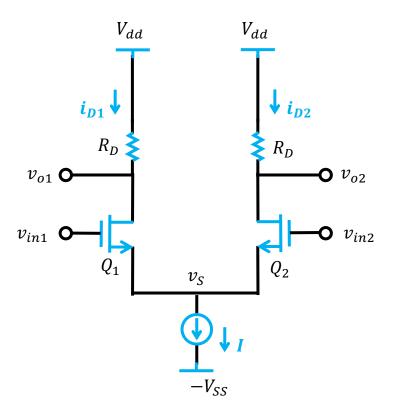
Step 2: perform AC analysis

$$v_{o1} = -g_m \frac{v_{id}}{2} (R_D || r_o)$$

 $v_{o2} = g_m \frac{v_{id}}{2} (R_D || r_o)$

$$v_o = v_{o2} - v_{o1} = -g_m v_{id}(R_D || r_o)$$

Summary: Differential Pair



DEFINE COMMON MODE VOLTAGE

$$\boldsymbol{V_{iCM}} \equiv \frac{1}{2}(v_{in1} + v_{in2})$$

DEFINE **DIFFERENTIAL MODE VOLTAGE**

$$v_{id} \equiv v_{in1} - v_{in2}$$

The voltage gain

$$|A_{CM}| = \frac{v_{o2} - v_{o1}}{v_{iCM}} = 0$$

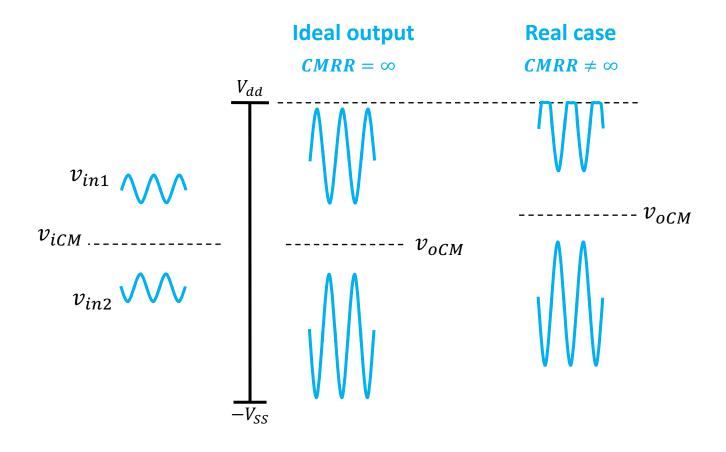
$$|A_d| = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m(R_D||r_o)$$

DEFINE COMMON MODE REJECTION RATIO

$$CMRR \equiv \left| \frac{A_d}{A_{CM}} \right| \xrightarrow{Ideally} \infty$$

Summary: Differential Pair

Why we need CMRR?
$$CMRR \equiv \left| \frac{A_d}{A_{CM}} \right| \xrightarrow{Ideally} \infty$$



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 - AC analysis techniques
 - The frequency response
- MOSFET v.s. BJT
- More examples of useful modules
 - Current sources
 - The MOS differential pair

Reading tasks & learning goals

- Reading tasks
 - Microelectronic Circuits, 6th edition
 - Chapter 5, 7.4.2–7.5, 8.1–8.2.2, 9.1–9.3
- Learning goals
 - Know the structure of a MOSFET and how it works
 - Well understand the characteristic of MOSFET
 - Well understand how to locate the bias point of a MOSFET in circuit
 - Well understand how to analyze a circuit with MOSFET
 - Well understand the similarity and difference between BJT and MOSFET
 - Well understand the MOSFET amplification circuit configuration and analysis
 - Know the fundamental analysis on current source and differential pairs