电子电路与系统基础

习题课第十一讲

1、第八周作业讲解
2、第九周作业讲解
3、单管放大器实验电路说明

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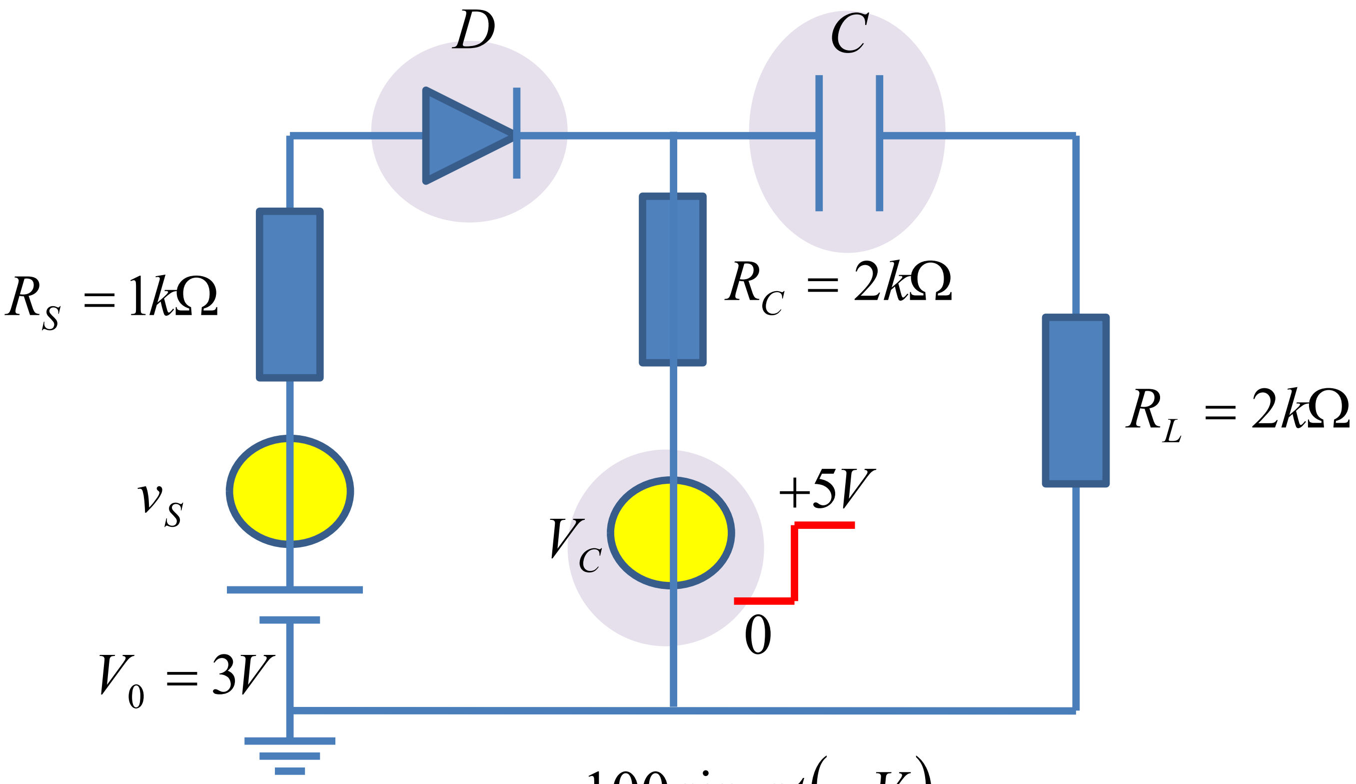
习题课第十一讲 大纲

- 第八周作业讲解
- 第九周作业讲解
- 单管放大器实验电路说明

第8周作业
作业3：二极管开关

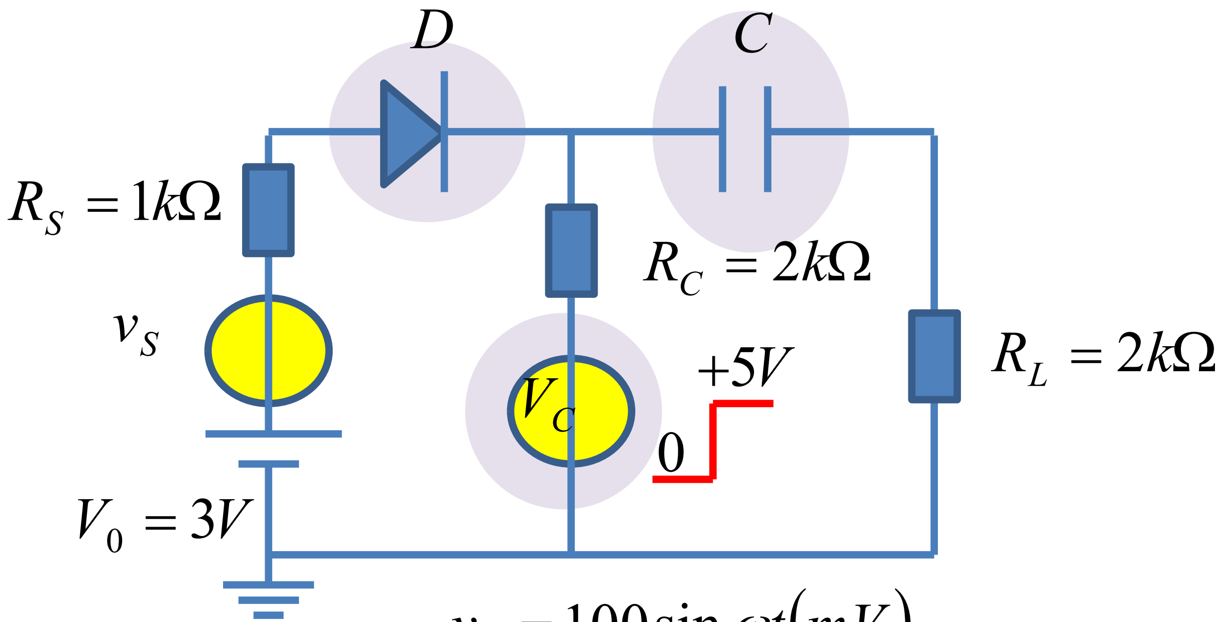
- 如图所示为二极管开关控制的信号传输电路，这里假设电容对直流信号是开路的，对交流小信号是短路的，分别求出控制电压**Vc**为**0V**和**5V**时的输出电压v_L波形
  - 分别画出直流等效电路和交流等效电路
    - 二极管直流模型：正偏**0.7V**电压源，反偏开路
    - 二极管交流模型：正偏短路，反偏开路



$$v_S = 100\sin\omega t(mV)$$

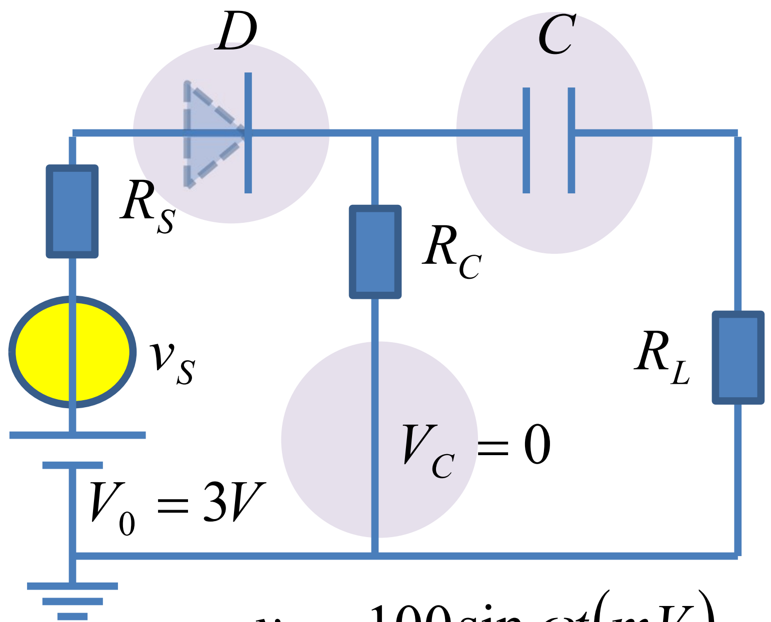
叠加定理不适用于非线性电路，直流分析是非线性分析
交流小信号在直流基础上起作用，是线性分析

二极管分段线性

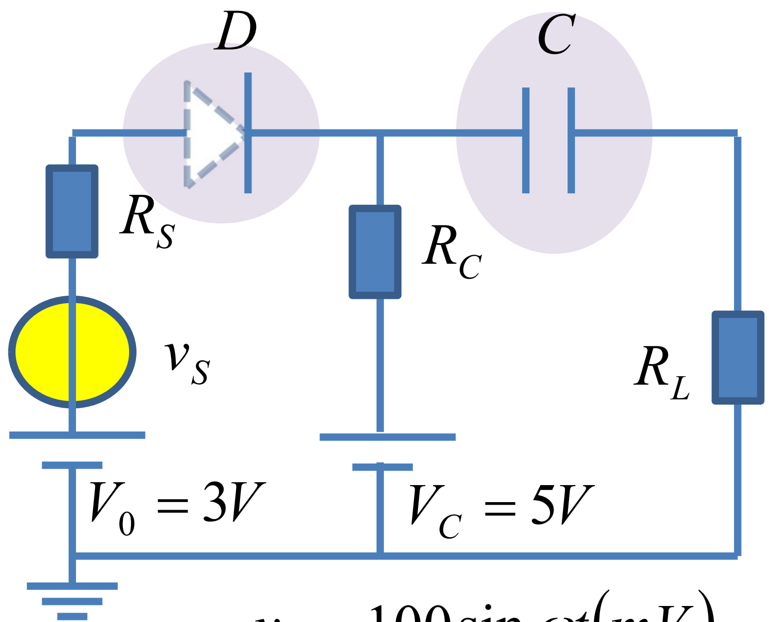


$$v_S = 100\sin\omega t\,(mV)$$

首要判定其工作区



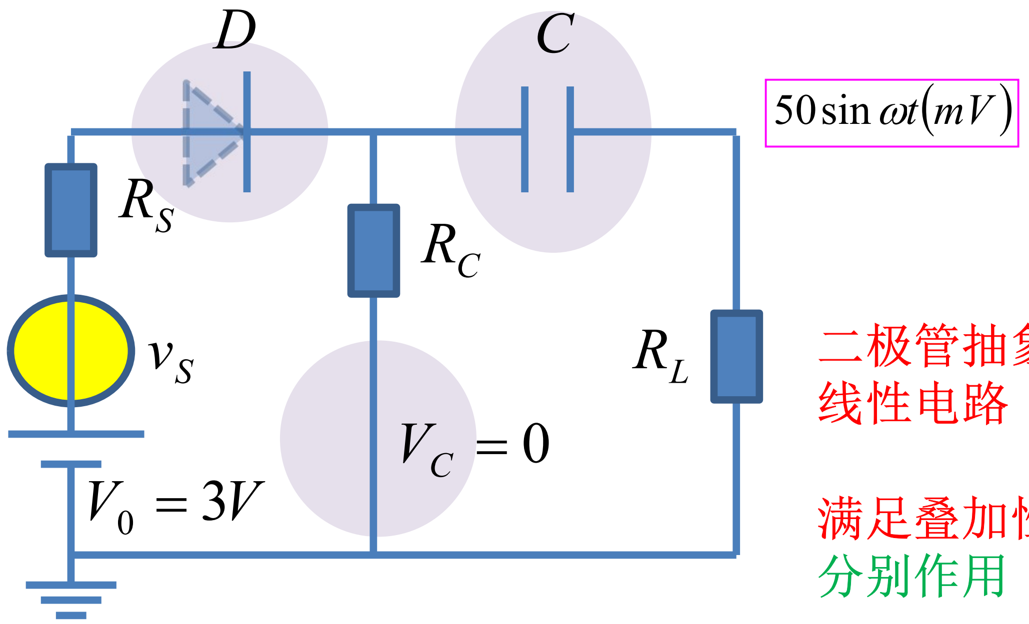
$$v_S = 100\sin\omega t\,(mV)$$



$$v_S = 100\sin\omega t\,(mV)$$

控制电压使导通

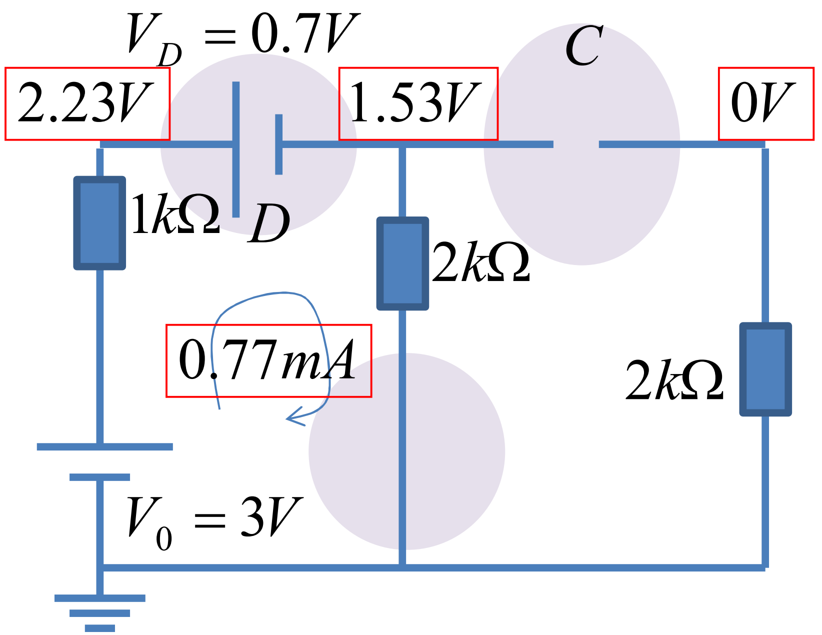
二极管导通，直接采用**0.7V**恒压源模型：二极管直流电流在**mA**量级，微分电阻在**10Ω**量级，和负载电阻比可认为短路



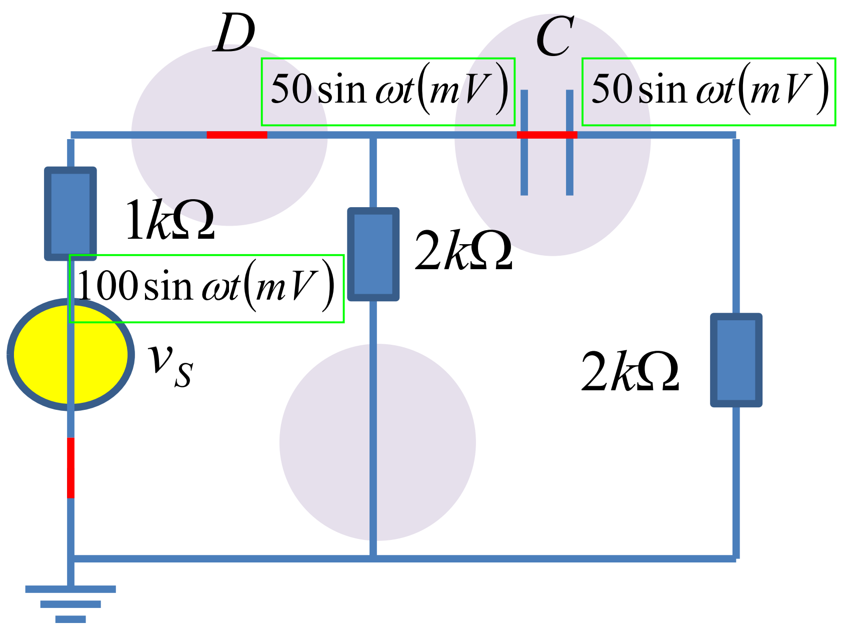
二极管抽象为恒压源线性电路

满足叠加性

分别作用

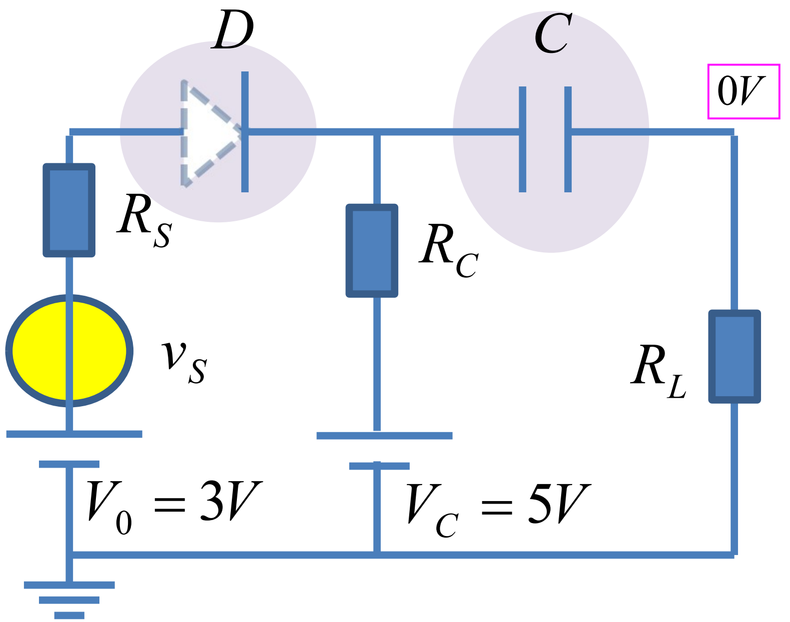


直流分析



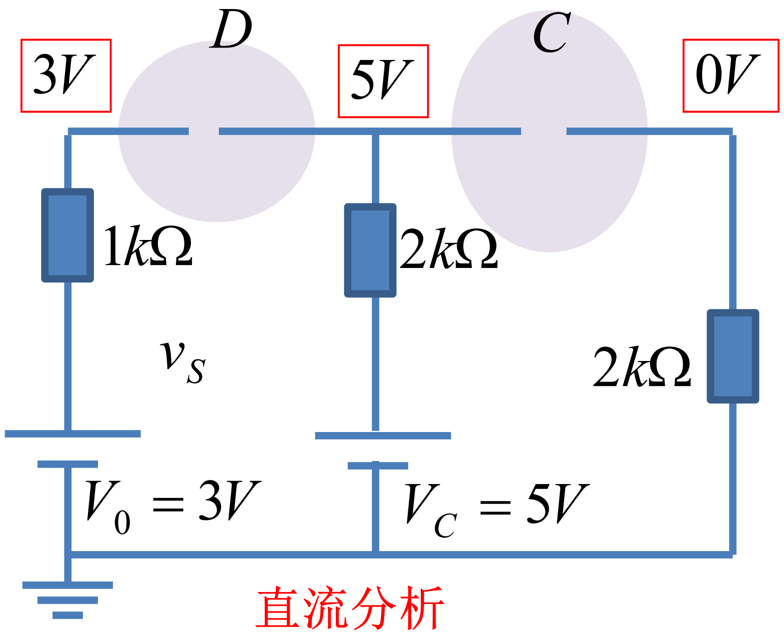
交流分析

控制电压使截止

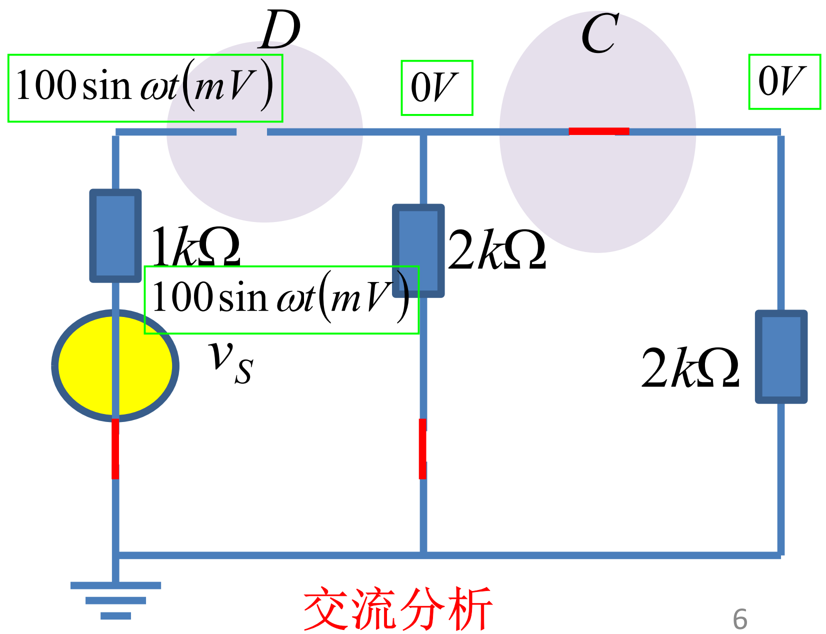


线性电路
满足叠加性

分别作用



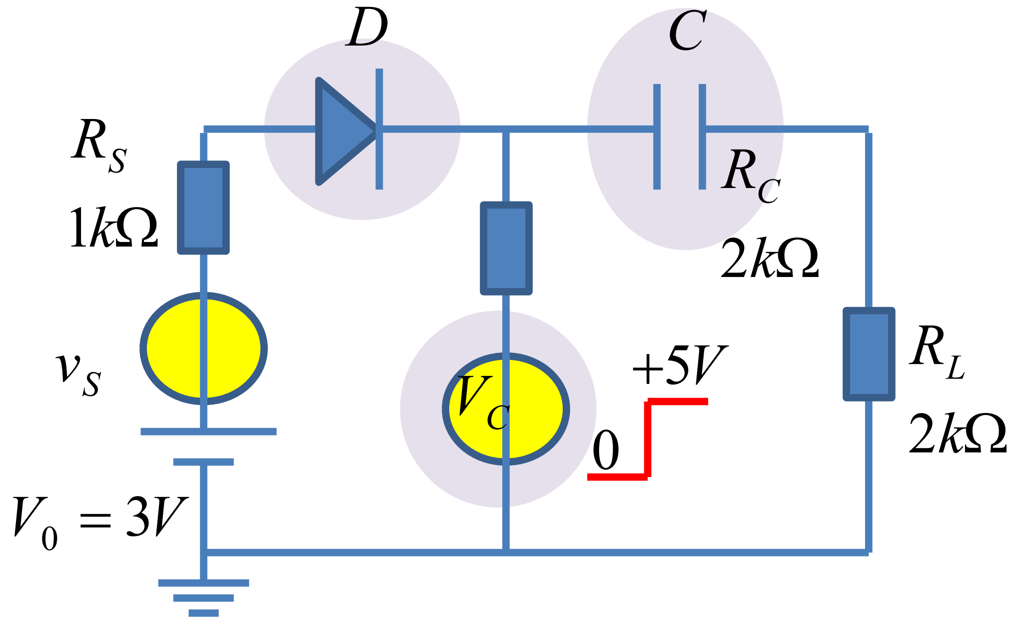
直流分析

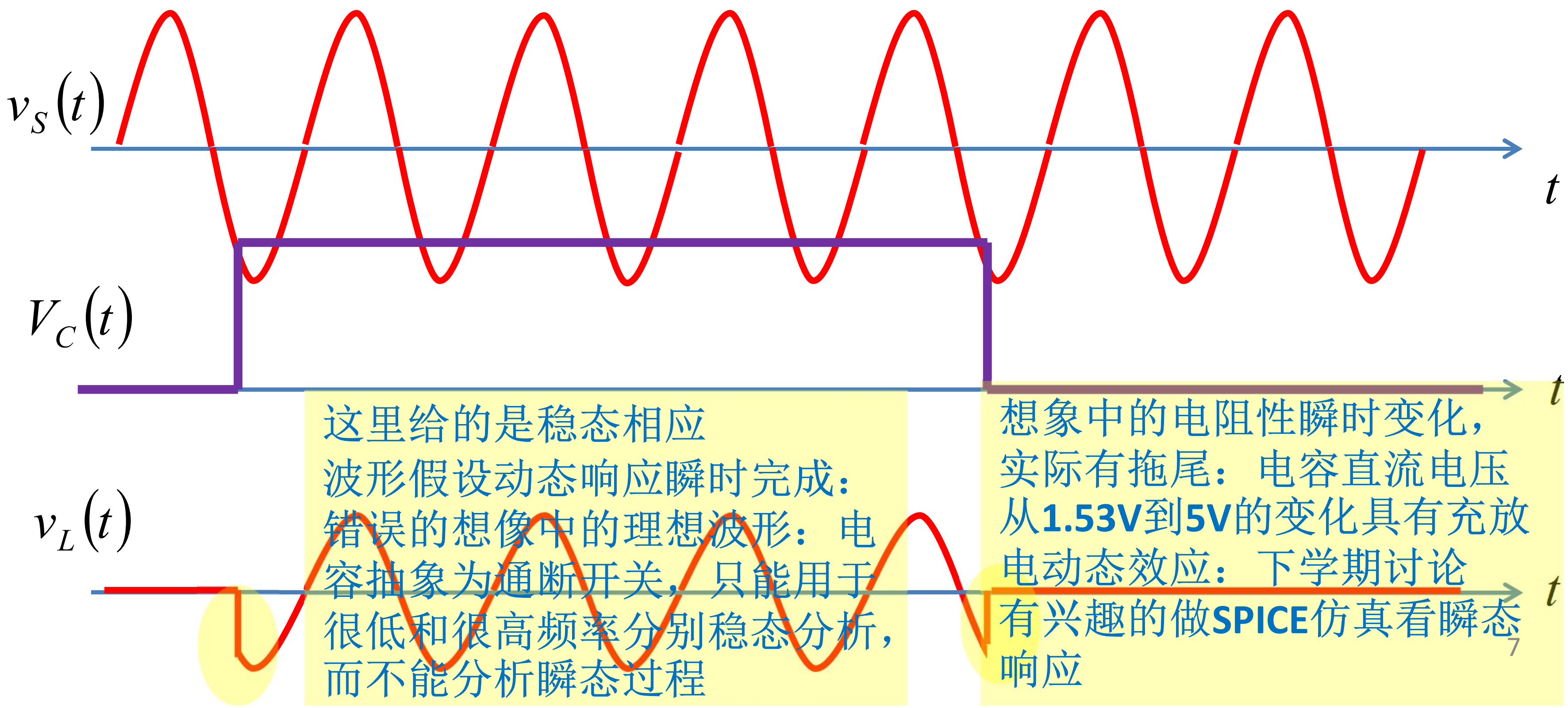


交流分析

输入输出波形

$$v_S = 100\sin\omega t(mV)$$





这里给的是稳态相应
波形假设动态响应瞬时完成：
错误的想像中的理想波形：电容抽象为通断开关，只能用于很低和很高频率分别稳态分析，而不能分析瞬态过程

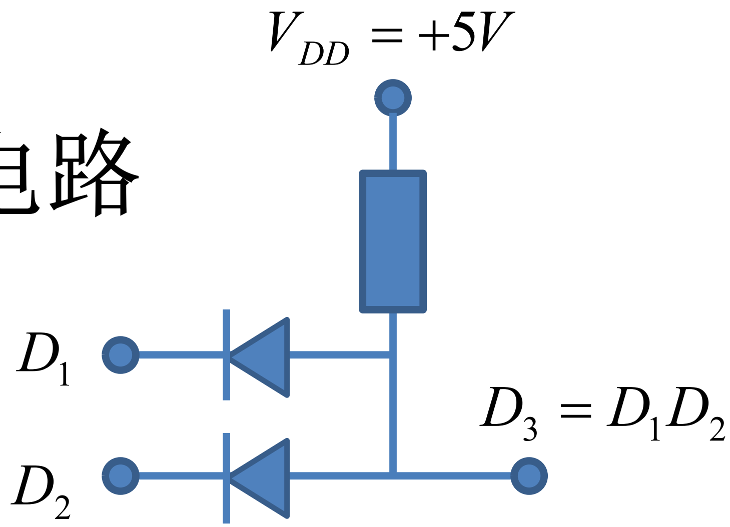
想象中的电阻性瞬时变化，实际有拖尾：电容直流电压从**1.53V**到**5V**的变化具有充放电动态效应：下学期讨论
有兴趣的做**SPICE**仿真看瞬态响应

第8周作业

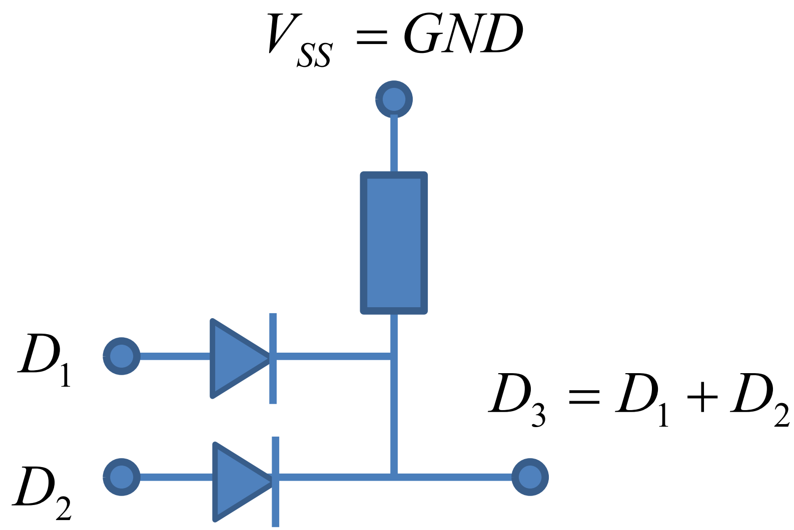
作业4：二极管数字门电路

- 我们将大于3V的电压视为逻辑状态1，将小于2V的电压视为逻辑状态0，2-3V的电压不定义其逻辑状态
  - （1）给出如下两个电路的输出逻辑状态
  - （2）用一句话说明逻辑与和逻辑或的逻辑运算规则（决策原则）
    - 其中逻辑1用‘同意’一词表述，逻辑0用‘不同意’一词表述
  - （3）回答：联合国安理会‘一票否决制’采用的是与运算还是或运算？

V_1（V）	V_2（V）	V_3（V）	D_1	D_2	D_3
0	0		0	0	
0	5		0	1	
5	0		1	0	
5	5		1	1	



与门：**and gate**



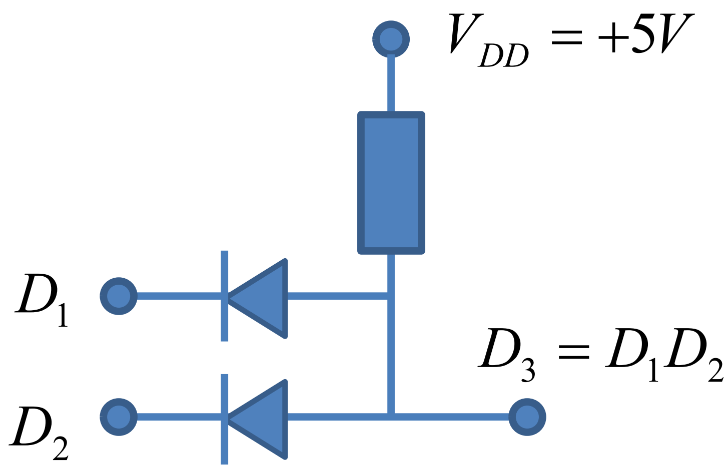
或门：**or gate**

二极管：一阶模型

与门、或门逻辑

V_1（v）	V_2（v）	V_3（v）	D_1	D_2	D_3
0	0	0.7	0	0	0
0	5	0.7	0	1	0
5	0	0.7	1	0	0
5	5	4.3	1	1	1

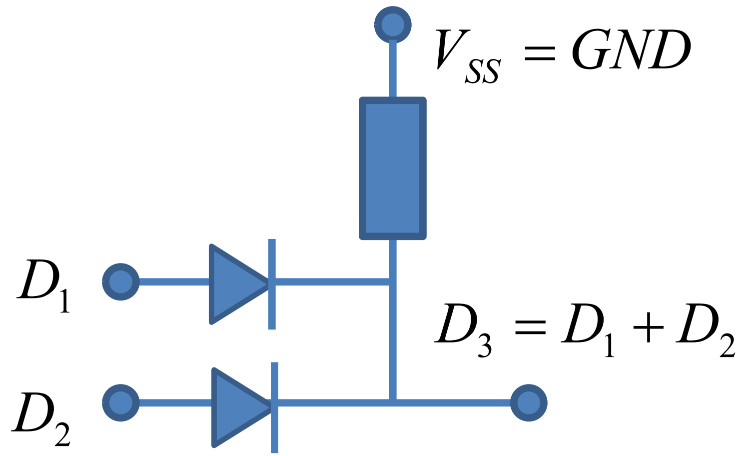
两个都同意方可通过



与门：**and gate**

V_1（v）	V_2（v）	V_3（v）	D_1	D_2	D_3
0	0	0	0	0	0
0	5	4.3	0	1	1
5	0	4.3	1	0	1
5	5	4.3	1	1	1

有一个同意即可通过

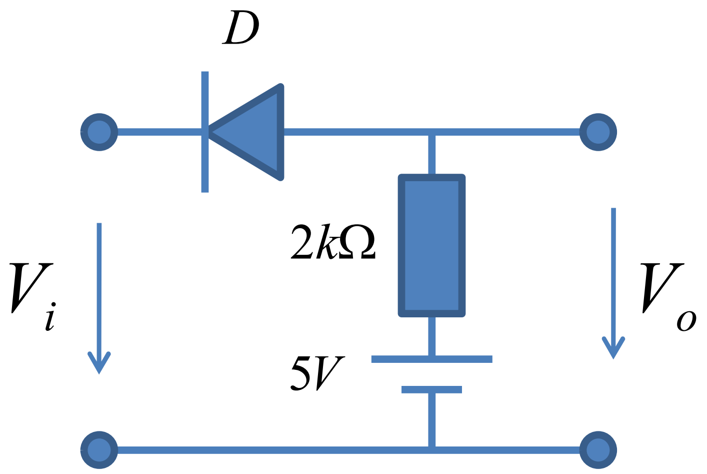


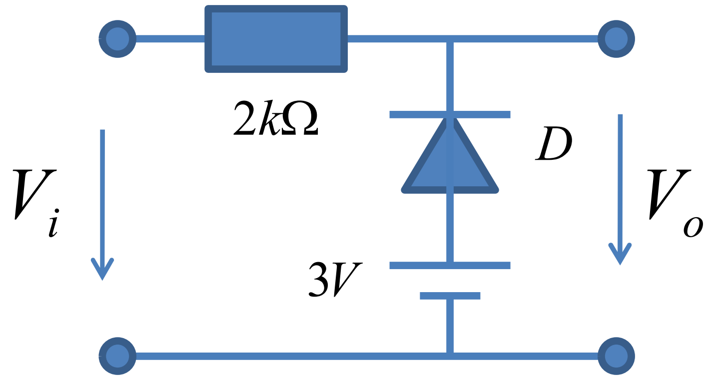
或门：**or gate**

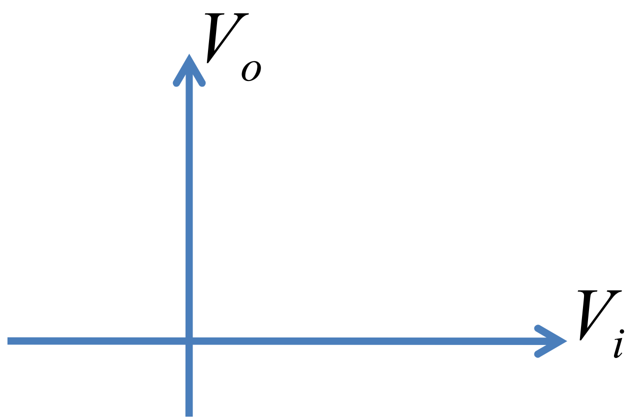
作业5 转移特性

作业中，普通**PN**结二极管均采用一阶模型：开关**+0.7V**偏压

- 画出如图所示电路的电压转移特性曲线

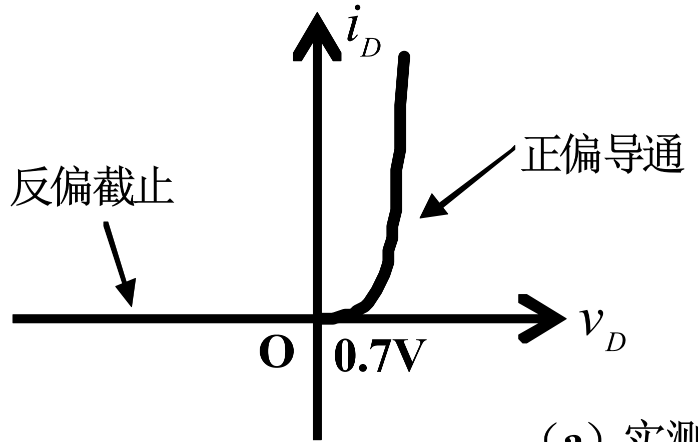




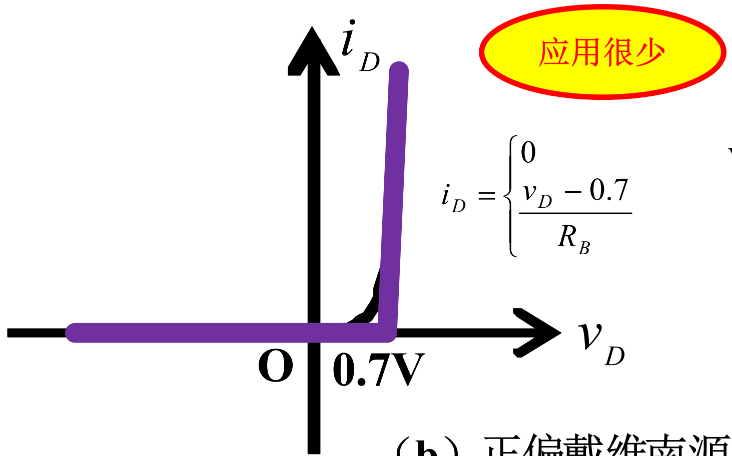


二极管模型

串接负载很小时，戴维南源内阻才会被考虑在内

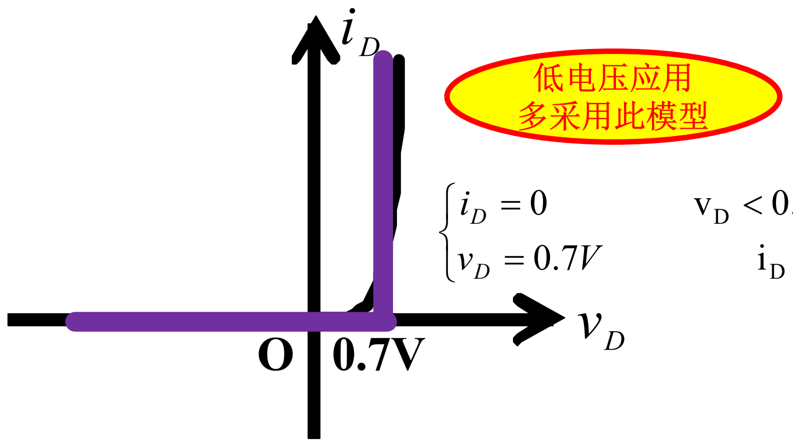


（a）实测特性



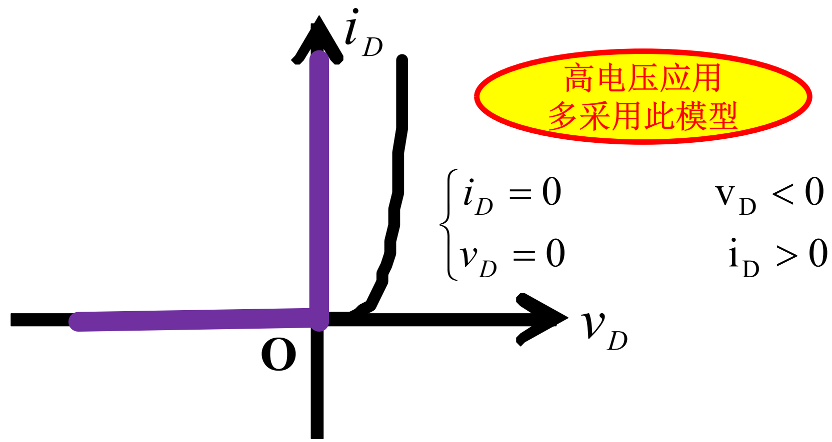
$$i_D=\begin{cases}0 & \mathrm{v_D}<0.7V\\ \dfrac{v_D-0.7}{R_B} & \mathrm{i_D}>0\end{cases}$$

（b）正偏戴维南源模型



$$\begin{cases}i_D=0 & \mathrm{v_D}<0.7V\\ v_D=0.7V & \mathrm{i_D}>0\end{cases}$$

（c）正偏恒压源模型



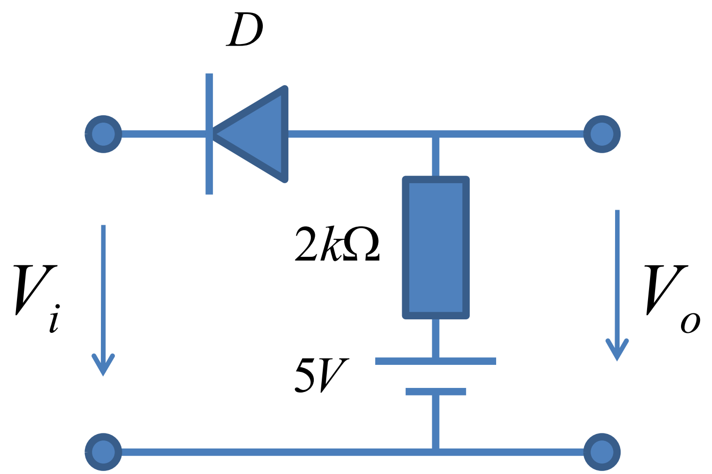
$$\begin{cases}i_D=0 & \mathrm{v_D}<0\\ v_D=0 & \mathrm{i_D}>0\end{cases}$$

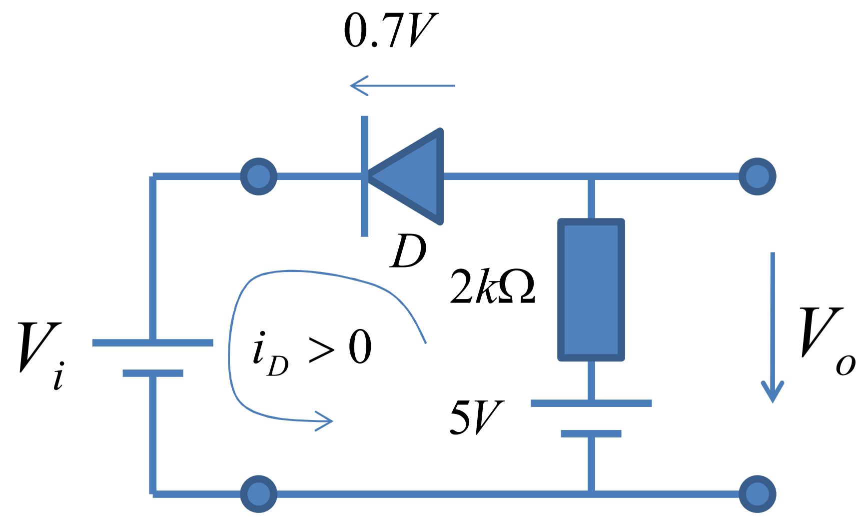
（d）理想整流模型

二极管分段折线

正偏导通，反偏截止

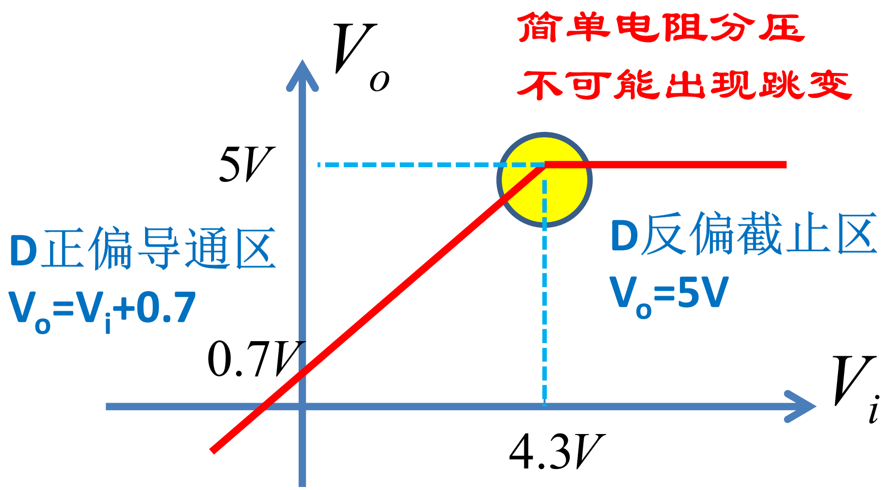
- 分界判断





假设D正偏导通，则$V_o=V_i+0.7$

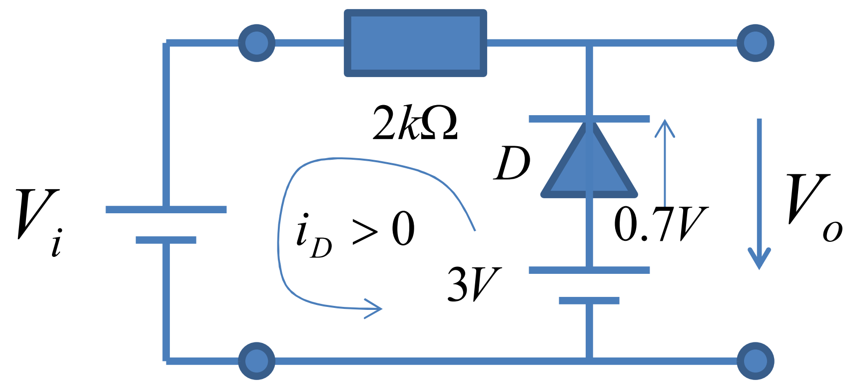
$$i_D = \frac{5-0.7-V_i}{R} > 0 \qquad V_i < 4.3V$$



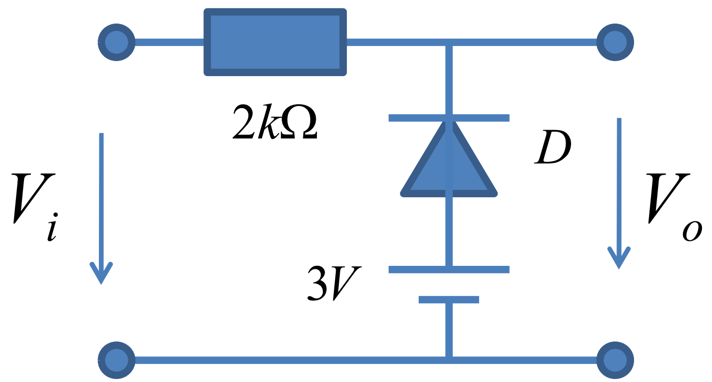
二极管分段折线

正偏导通，反偏截止

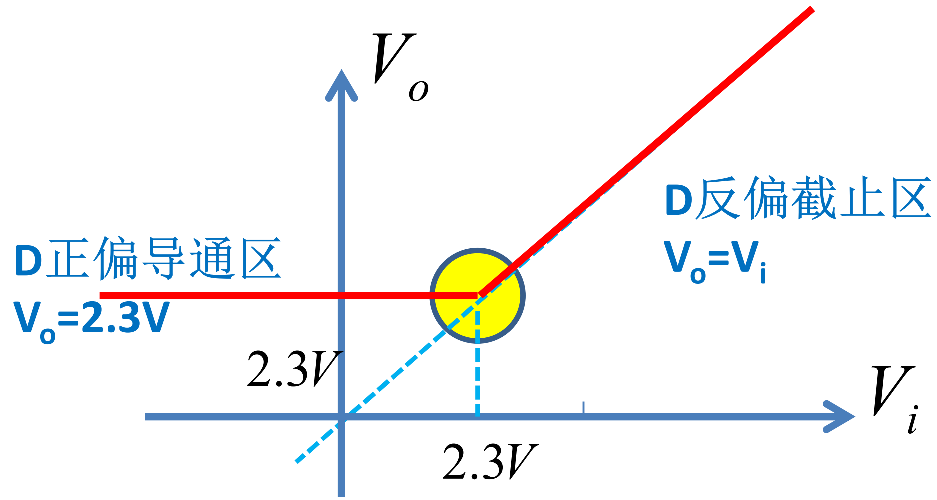
- 分界判断



假设D正偏导通，则V_o=2.3V

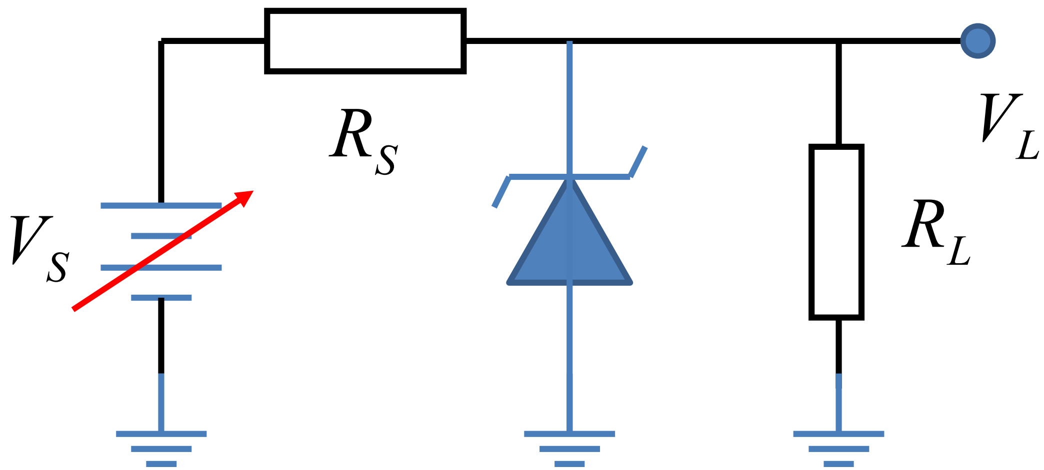


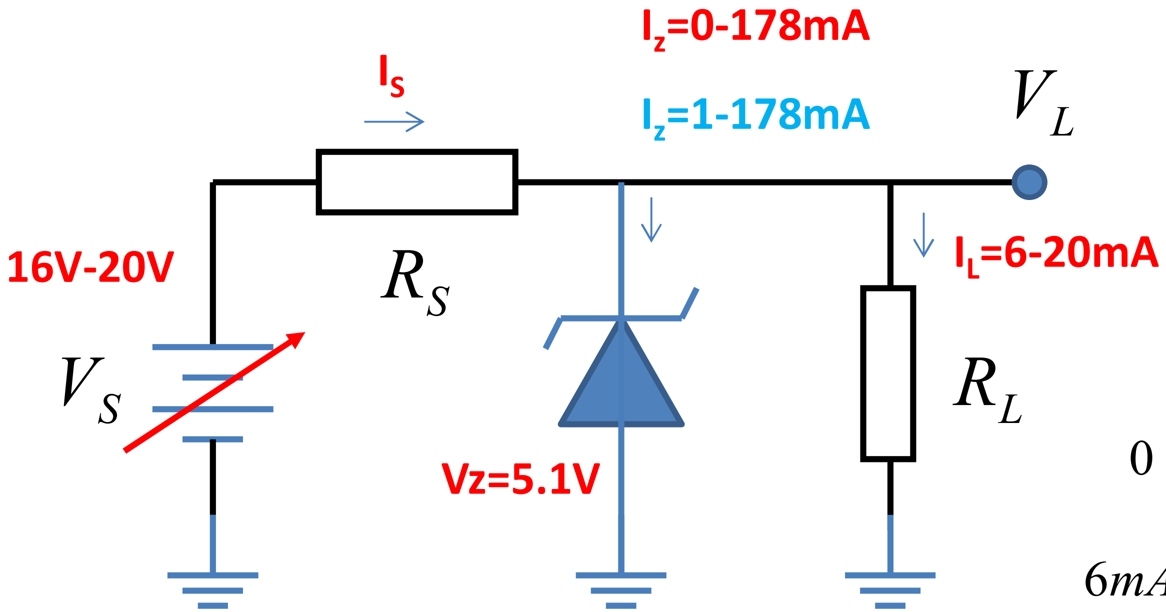
$$i_D = \frac{3-0.7-V_i}{R} > 0 \qquad V_i < 2.3V$$



作业6 二极管稳压器

- 一个齐纳稳压电路，输入电压在**16V-20V**之间变动，齐纳二极管为**1N4733A**，负载电阻$\mathbf{R_L}$要求负载电流为**6mA-20mA**才能正常工作，限流电阻$\mathbf{R_S}$的取值范围是多少？
  - 齐纳二极管采用理想电压源模型，反向击穿假设为**5.1V**恒压
  - 当输入电压、限流电阻、负载电流都取中间值时，求所有元件上释放或消耗的功率大小





$$0 < I_Z < 178mA$$

$$6mA < I_L < 20mA$$

$$I_Z + I_L = I_S = \frac{V_S - V_Z}{R_S}$$

$$6 \sim 20mA = I_L < \frac{V_S - V_Z}{R_S} < 178 + I_L = 184 \sim 198mA$$

$$20mA < \frac{V_S - V_Z}{R_S} < 184mA$$

$$59 \sim 81\Omega = \frac{(16 \sim 20) - 5.1}{184mA} = \frac{V_S - V_Z}{184mA} < R_S < \frac{V_S - V_Z}{20mA} = \frac{(16 \sim 20) - 5.1}{20mA} = 545 \sim 745\Omega$$

$$81\Omega < R_S < 545\Omega$$

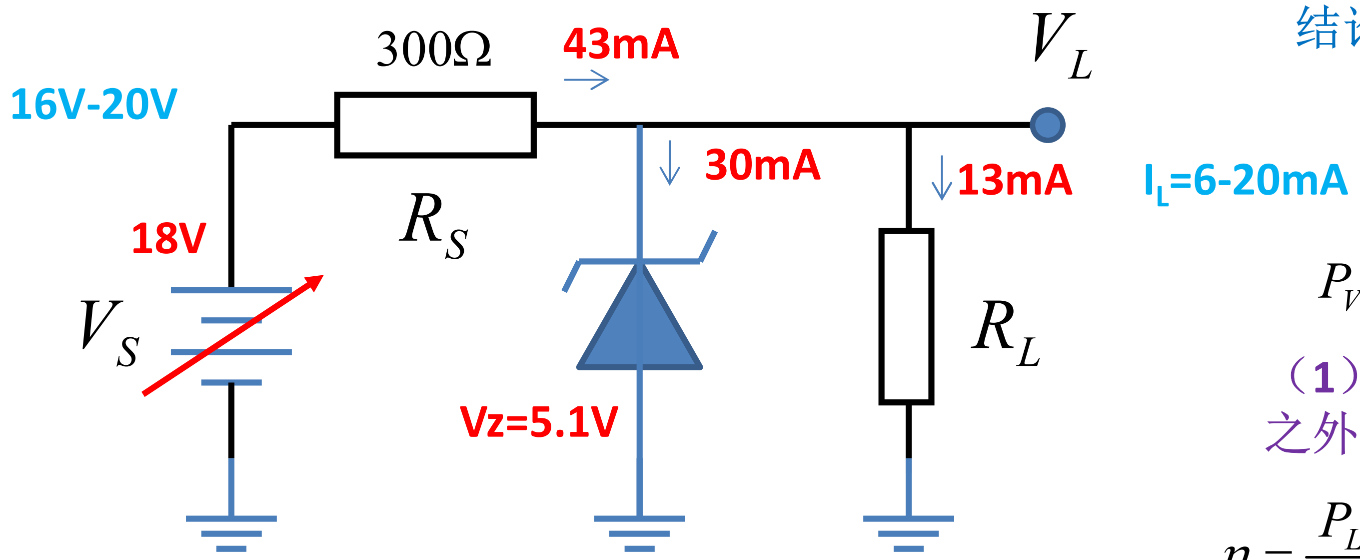
$$81\Omega < R_S < 519\Omega$$

功率分配情况

$81\Omega < R_S < 545\Omega$　　$81\Omega < R_S < 519\Omega$

$R_S = 313\Omega$

结论差不多，自算



$$P_{V_S} = P_{R_S} + P_D + P_L$$

（1）能量守恒：电源之外都是阻性器件

$$\eta = \frac{P_L}{P_{V_S}} = \frac{66.3}{774} = 8.57\%$$

（2）效率很低

（3）负载端口向内部看，齐纳二极管提供的是恒压特性，V_S则提供能量，整体等效为5.1V恒压源

$$I_S = \frac{V_S - V_Z}{R_S} = \frac{18-5.1}{300} = 0.043A = 43mA$$

$$I_R = I_S - I_L = 43 - 13 = 30mA$$

$$P_{V_S} = V_S I_S = 18V \times 43mA = 774mW$$ 源释放功率

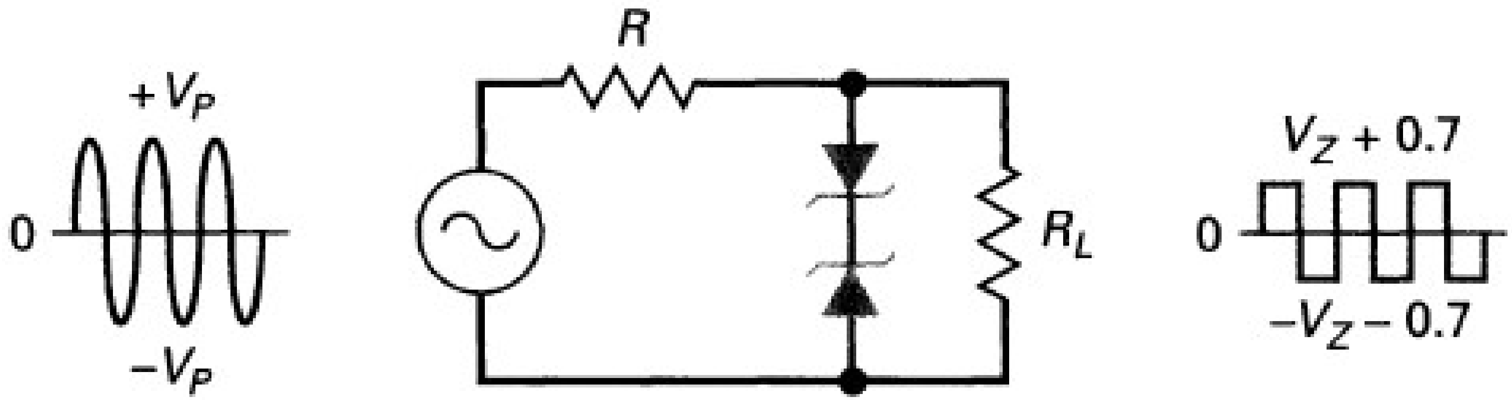
$$P_{R_S} = I_S^2 R_S = (43mA)^2 \times 300\Omega = 554.7mW$$ 限流电阻耗能

$$P_D = V_Z I_Z = 5.1V \times 30mA = 153mW$$ 齐纳二极管耗能

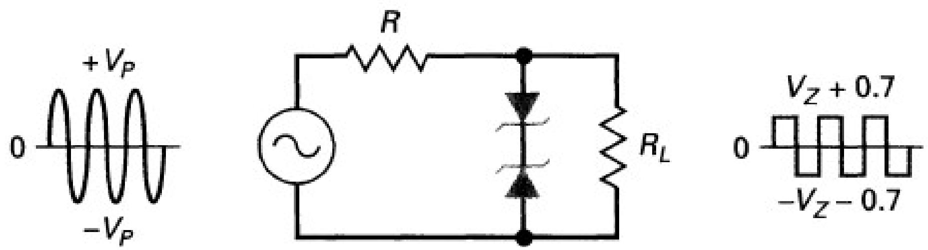
$$P_L = V_Z I_Z = 5.1V \times 13mA = 66.3mW$$ 负载电阻耗能

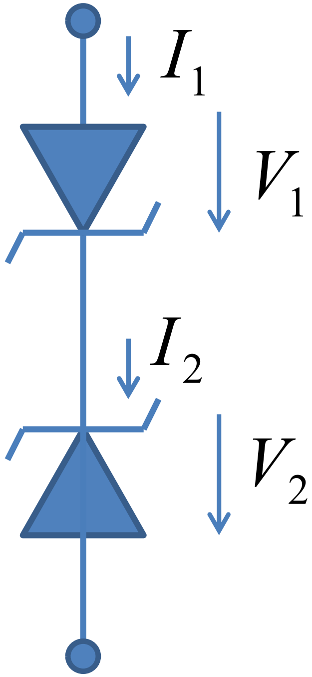
作业7 限幅器

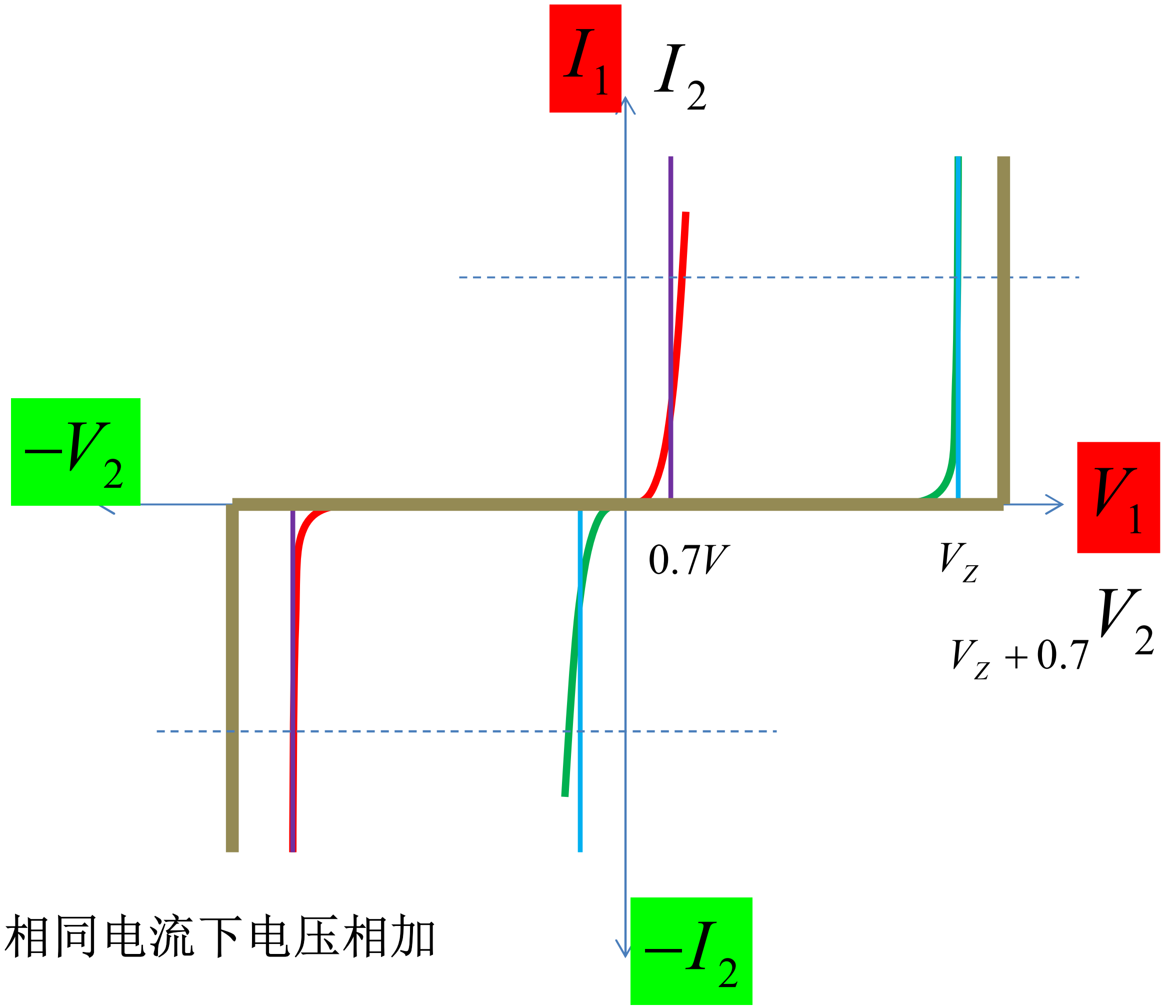
- 分析说明图示电路为什么有这样的输出电压波形？



稳压二极管串接

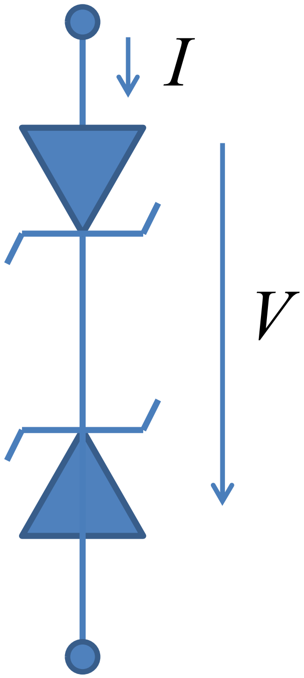


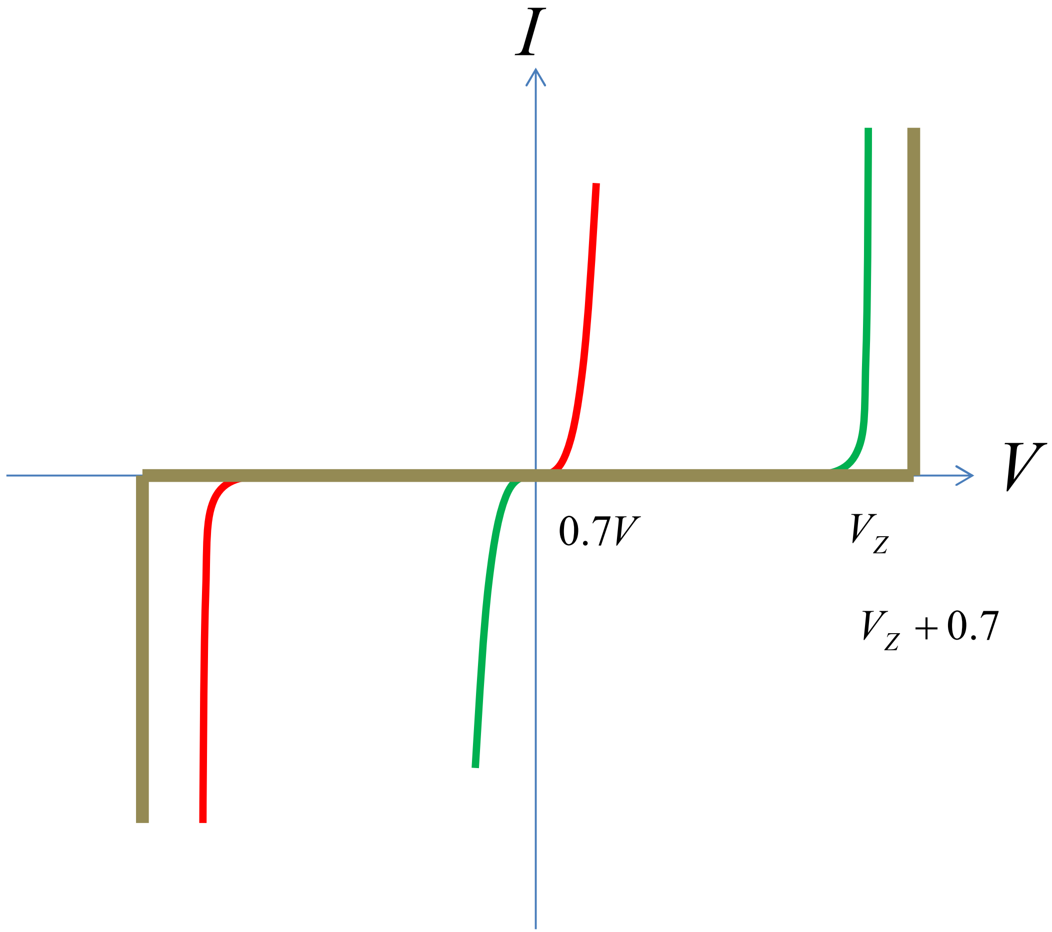




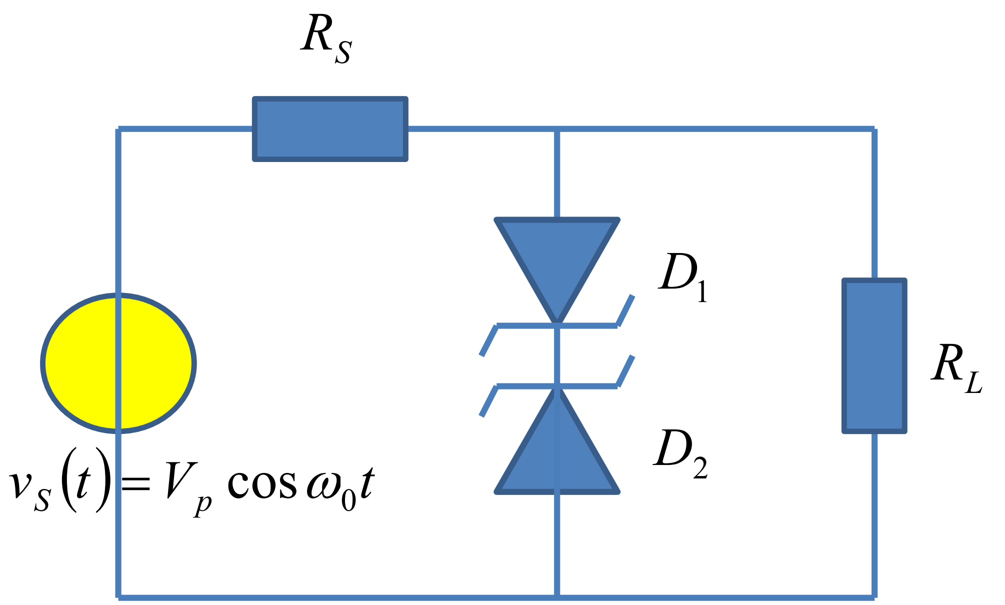
串联：相同电流下电压相加

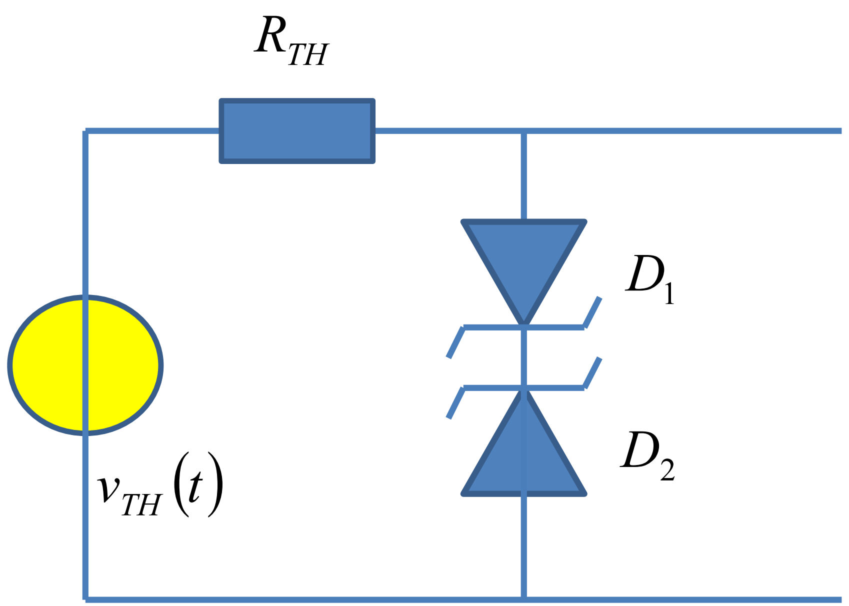
分段折线电路模型





$$\begin{cases} V=+V_Z+0.7 & I>0 & \text{恒压源} \\ I=0 & -V_Z-0.7<V<+V_Z+0.7 & \text{开路} \\ V=-V_Z-0.7 & I<0 & \text{恒压源} \end{cases}$$



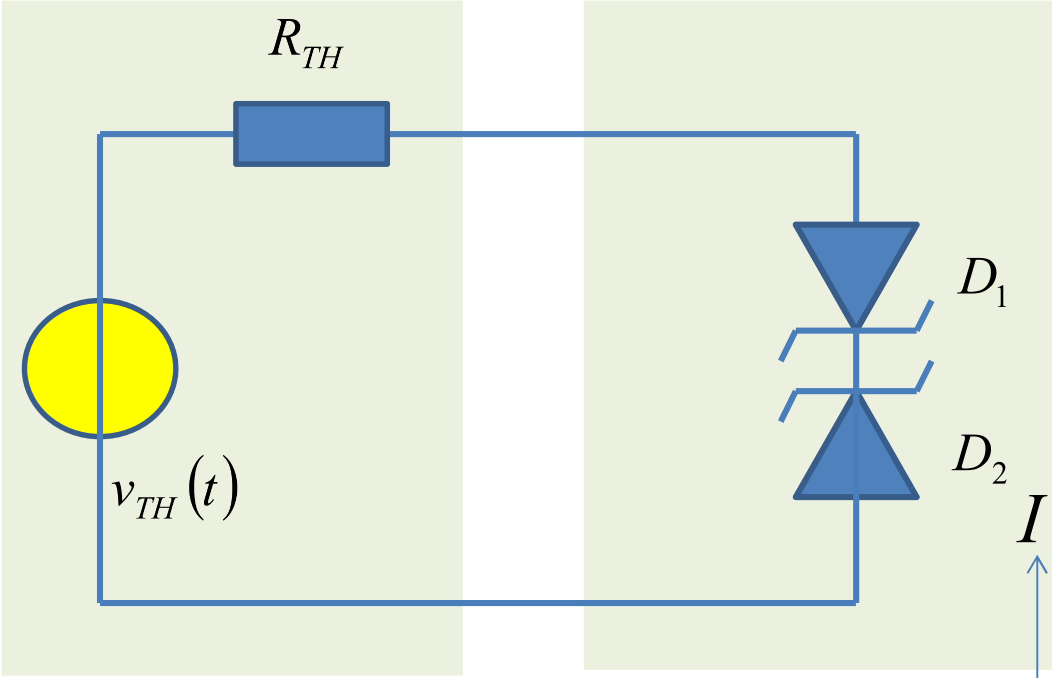


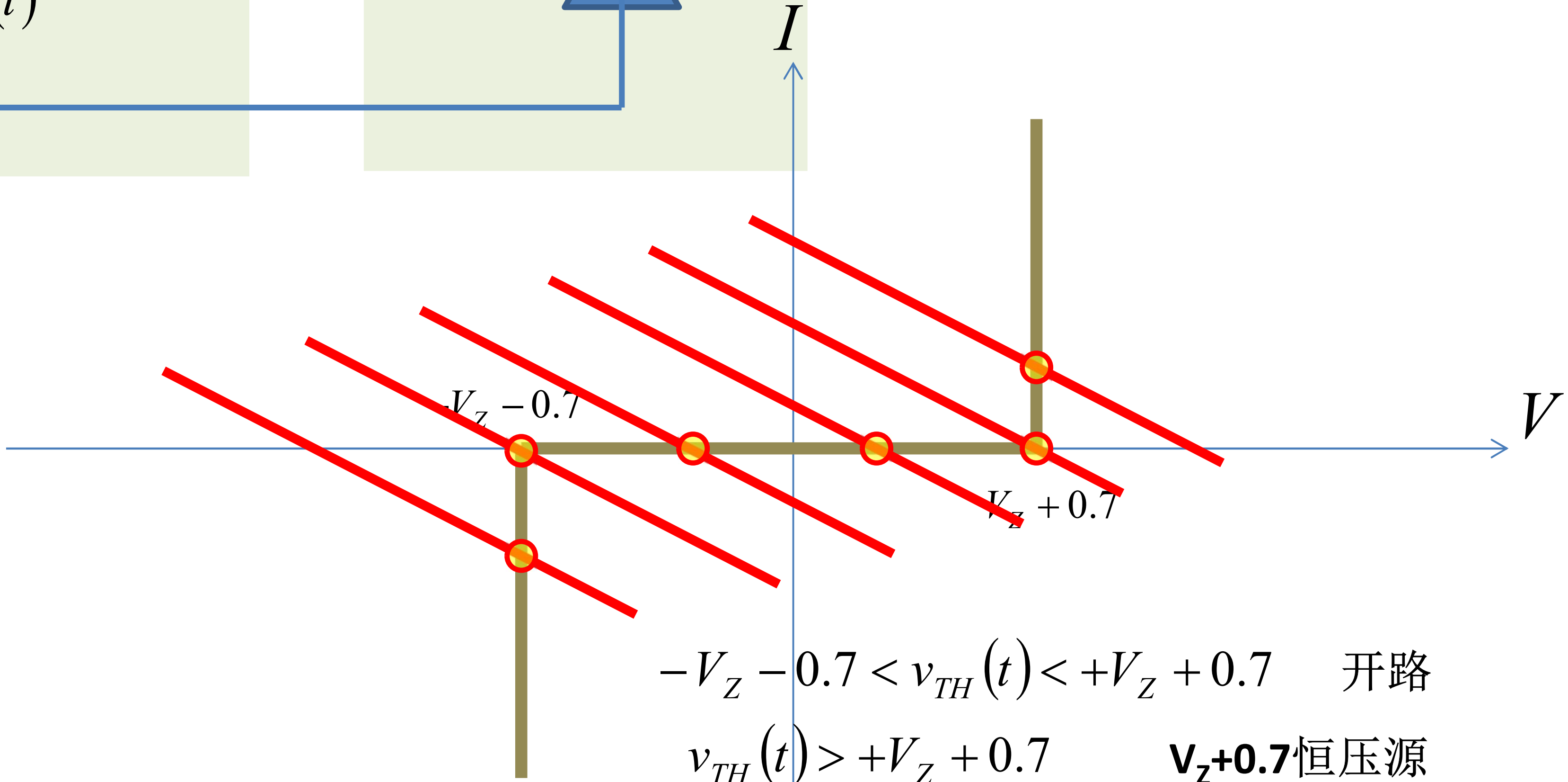
$$v_{TH}(t) = \frac{R_L}{R_L + R_S} v_S(t)$$

$$= \eta V_p \cos\omega_0 t$$

$$R_{TH} = \frac{R_L R_S}{R_L + R_S}$$

图解法理解

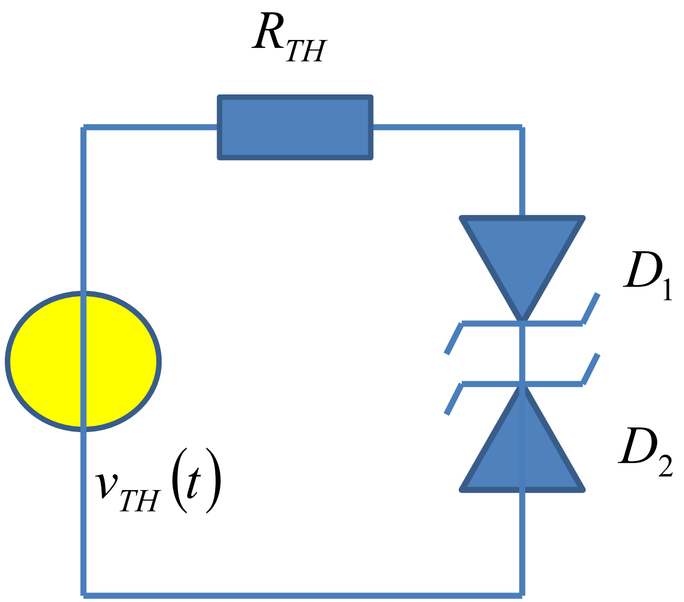




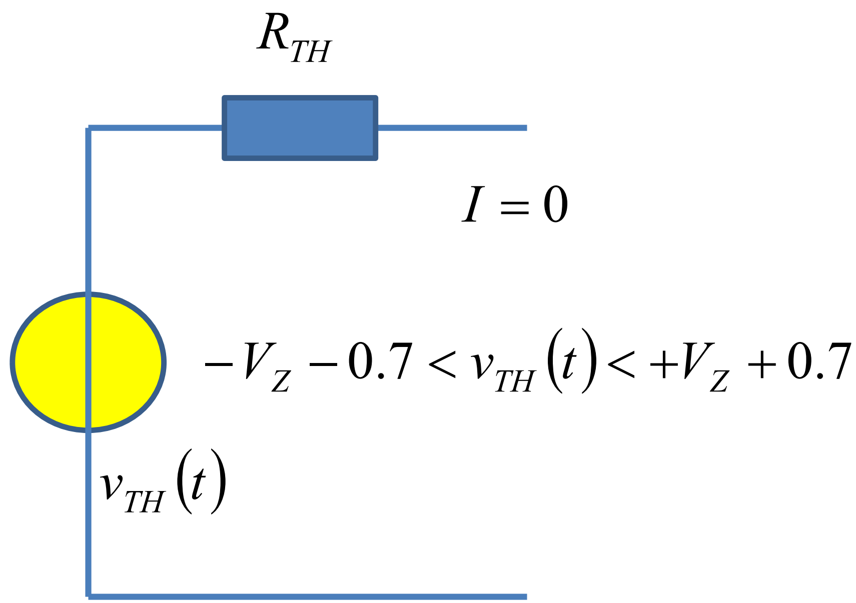
$-V_Z-0.7<v_{TH}(t)<+V_Z+0.7$ 开路

$v_{TH}(t)>+V_Z+0.7$ **V_Z+0.7恒压源**

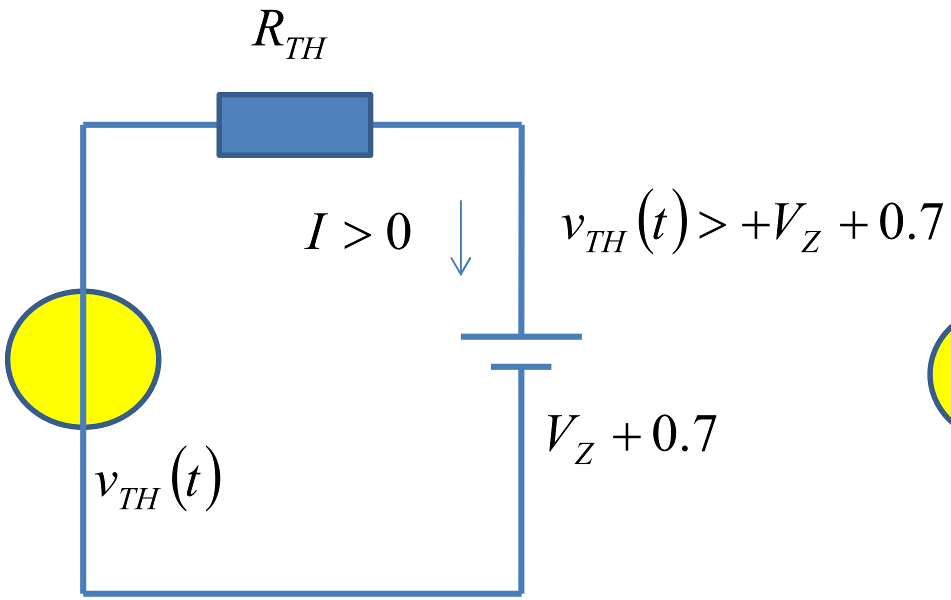
$v_{TH}(t)<-V_Z-0.7$ **-V_Z-0.7恒压源**



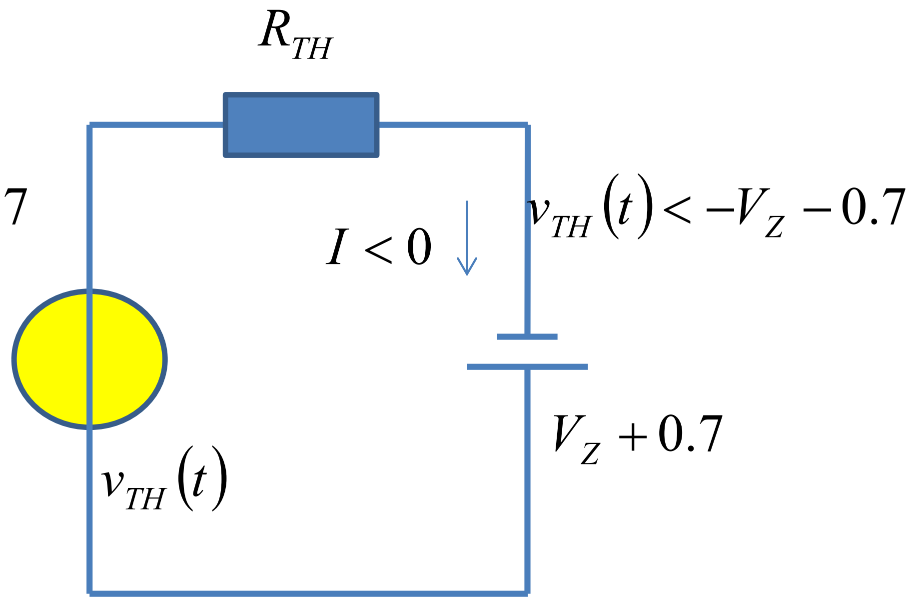
R_{TH}
D_1
D_2
$v_{TH}(t)$



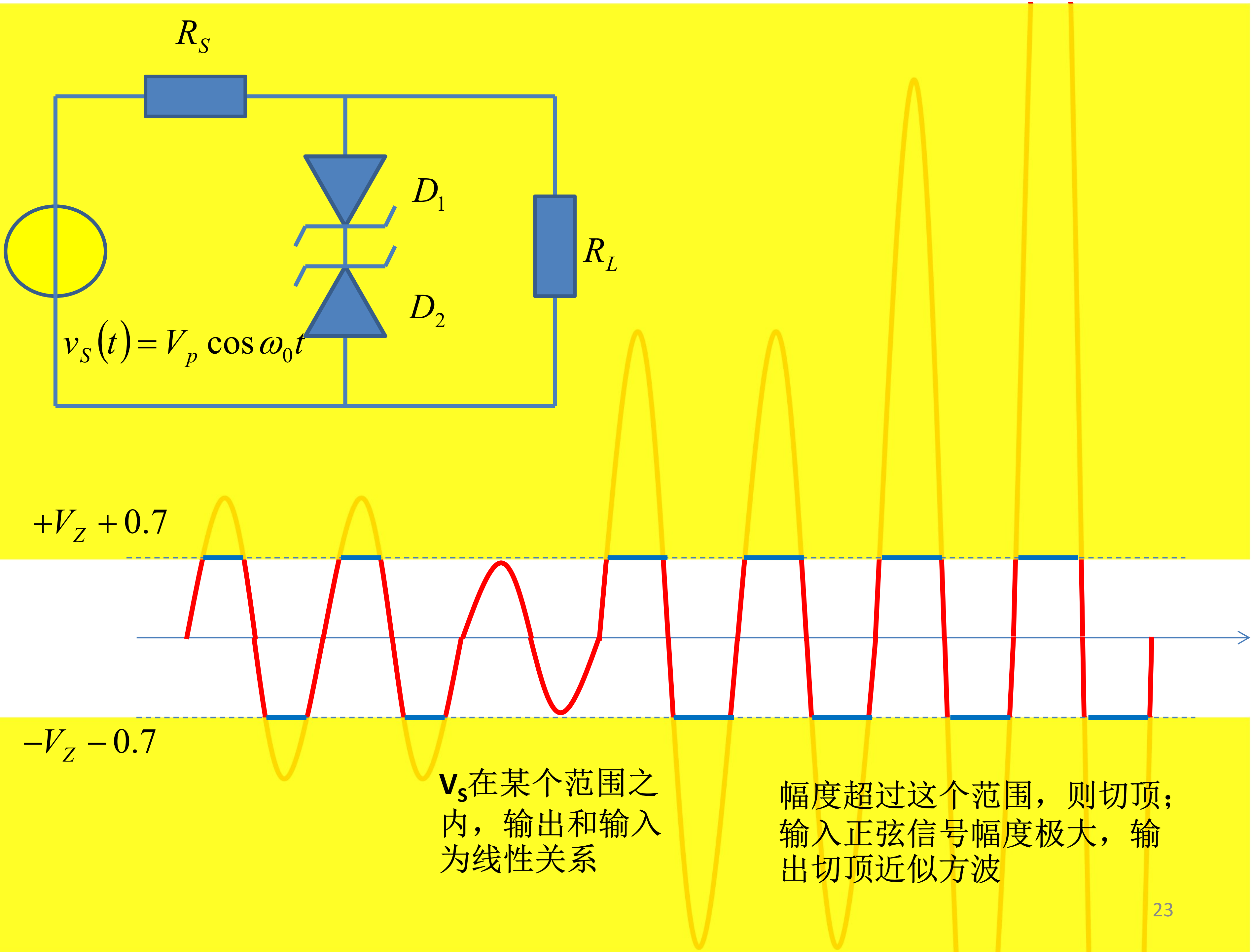
R_{TH}
$I=0$
$-V_Z-0.7<v_{TH}(t)<+V_Z+0.7$
$v_{TH}(t)$



R_{TH}
$I>0$
$v_{TH}(t)>+V_Z+0.7$
$V_Z+0.7$
$v_{TH}(t)$



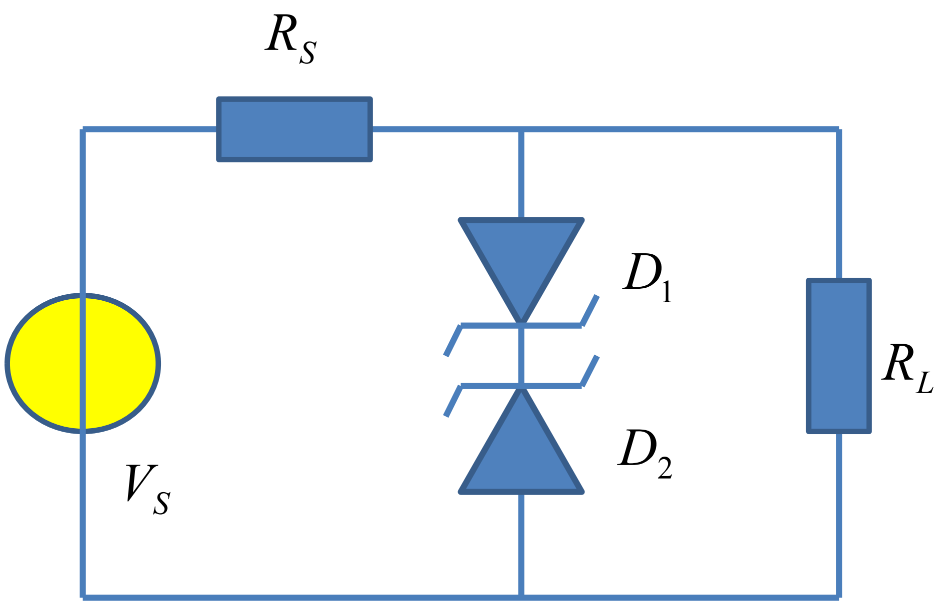
R_{TH}
$v_{TH}(t)<-V_Z-0.7$
$I<0$
$V_Z+0.7$
$v_{TH}(t)$

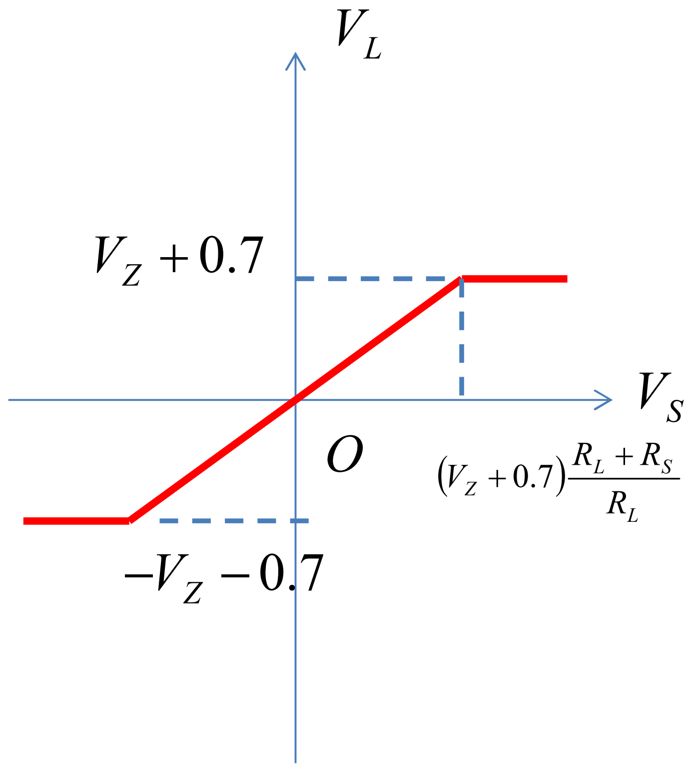


V_S在某个范围之内，输出和输入为线性关系

幅度超过这个范围，则切顶；输入正弦信号幅度极大，输出切顶近似方波

输入输出转移特性曲线

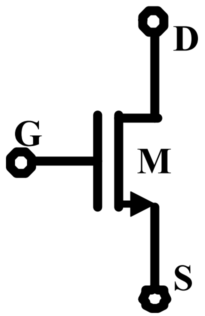


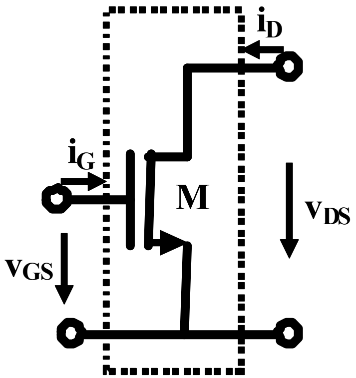


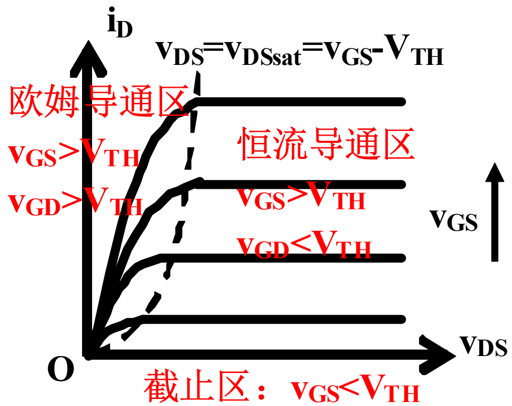
V_S在某个范围之内，输出和输入为线性关系；幅度超过这个范围，则切顶（饱和）

第9周作业1：NMOS晶体管

- （1）某NMOSFET的过驱动电压为0.5V，其饱和电压为多少？
- （2）该晶体管的β_n=2mA/V²，厄利电压为V_E=50V，则在V_{DS}=1V时，漏极电流为多少？
  - 必做：不考虑厄利效应；选作：考虑厄利效应
- （3）其等效电路模型中的源电流为多少？源内阻为多少？







- （1）某NMOSFET的过驱动电压为0.5V，其饱和电压为多少？
- （2）该晶体管的β_n=2mA/V²，厄利电压为V_E=50V，则在V_{DS}=1V时，漏极电流为多少？
- （3）其等效电路模型中的源电流为多少？源内阻为多少？

$V_{od} = V_{GS} - V_{TH} = 0.5V$ 过驱动电压：只有过驱动，$V_{GS}=V_{TH}+V_{od}$，才能有静电荷积累形成的沟道

从V_{GS}这个角度看：是否导通或者截止

$V_{DS,sat} = V_{GS} - V_{TH} = 0.5V$ 饱和电压：只要$V_{DS}>V_{DS,sat}$，沟道则夹断，电流呈现饱和特性

从V_{DS}这个角度看导通是欧姆导通还是恒流导通

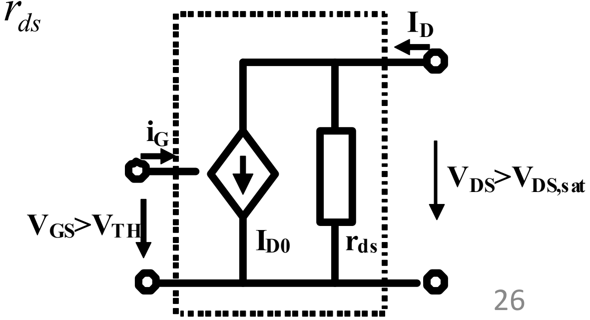
$V_{DS} = 1V > V_{DS,sat} = 0.5V$ 晶体管位于有源区

$$I_D = \beta_n (V_{GS} - V_{TH})^2 \left(1 + \frac{V_{DS}}{V_E}\right) = 2 \times 0.5^2 \times \left(1 + \frac{1}{50}\right) = 0.5 \times 1.02 = 0.51mA$$

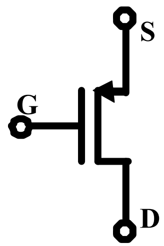
$$I_D = \beta_n (V_{GS} - V_{TH})^2 \left(1 + \frac{V_{DS}}{V_E}\right) = I_{D0}\left(1 + \frac{V_{DS}}{V_E}\right) = I_{D0} + \frac{V_{DS}}{V_E / I_{D0}} = I_{D0} + \frac{V_{DS}}{r_{ds}}$$

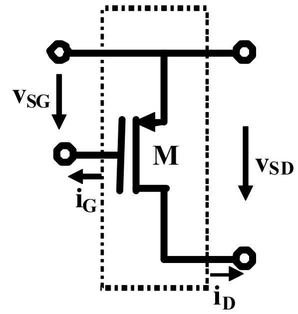
$$I_{D0} = \beta_n (V_{GS} - V_{TH})^2 = 2 \times 0.5^2 = 0.5mA$$

$$r_{ds} = \frac{V_E}{I_{D0}} = \frac{50V}{0.5mA} = 100k\Omega$$

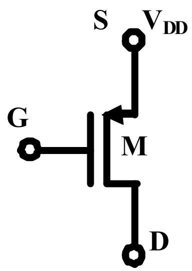


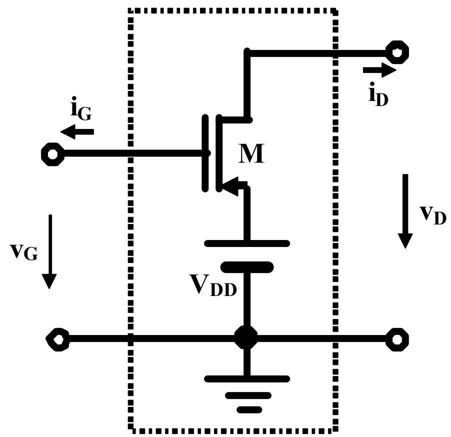
作业2：PMOS晶体管





- 画表格，一侧NMOS，一侧PMOS
- （1）画出NMOS、PMOS晶体管电路符号，二端口网络定义（端口电压、端口电流）
- （2）写出NMOS、PMOS晶体管的元件约束方程
- （3）画出伏安特性曲线示意图
- （4）对于图示的PMOS连接，给出二端口网络的元件约束方程，画出输出端口（有源负载）伏安特性曲线示意图

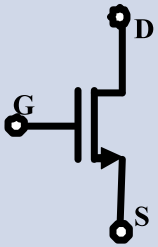
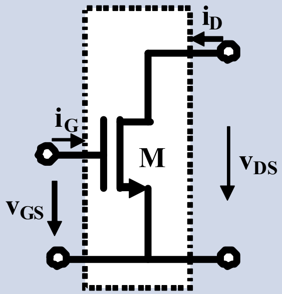
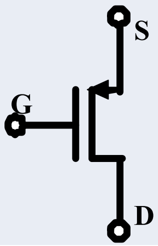
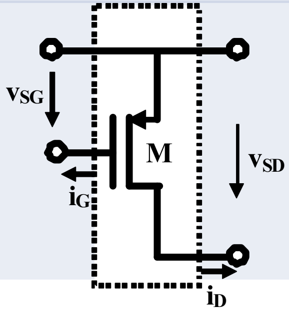


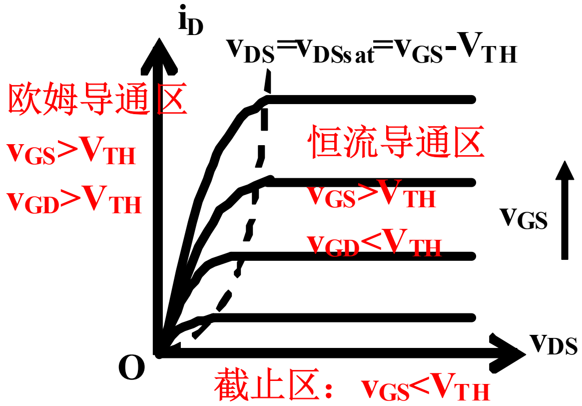


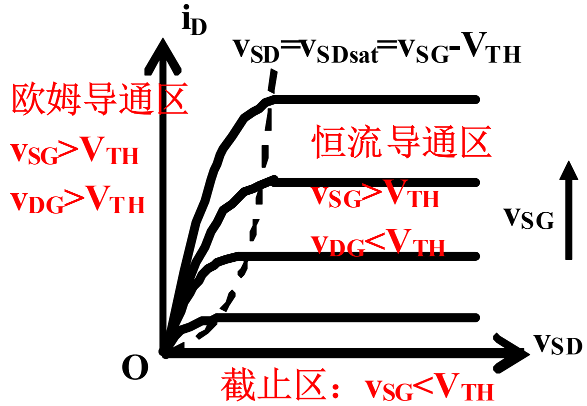
有源负载：可向外提供能量，具有非线性内阻的电压源，v_G固定则可作为NMOS的负载，v_G变化则可实现PMOS反相功能

源：源关联参考方向

NMOS和PMOS

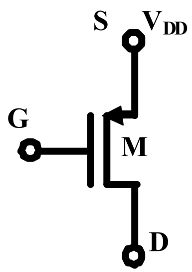
	电路符号	二端口网络定义	元件约束条件
NMOS			$i_D=\begin{cases}0 & v_{GS}<V_{TH,n}\\ 2\beta_n\left(\left(v_{GS}-V_{TH,n}\right)v_{DS}-0.5v_{DS}^2\right) & v_{GS}>V_{TH,n}, v_{GD}>V_{TH,n}\\ \beta_n\left(v_{GS}-V_{TH,n}\right)^2\left(1+\lambda_n v_{DS}\right) & v_{GS}>V_{TH,n}, v_{GD}<V_{TH,n}\end{cases}$
PMOS			$i_D=\begin{cases}0 & v_{SG}<V_{TH,p}\\ 2\beta_p\left(\left(v_{SG}-V_{TH,p}\right)v_{SD}-0.5v_{SD}^2\right) & v_{SG}>V_{TH,p}, v_{DG}>V_{TH,p}\\ \beta_p\left(v_{SG}-V_{TH,p}\right)^2\left(1+\lambda_p v_{SD}\right) & v_{SG}>V_{TH,p}, v_{DG}<V_{TH,p}\end{cases}$

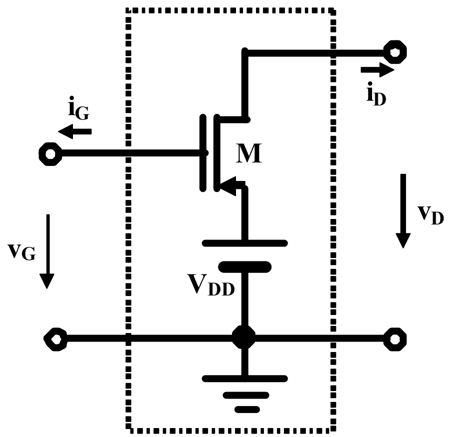




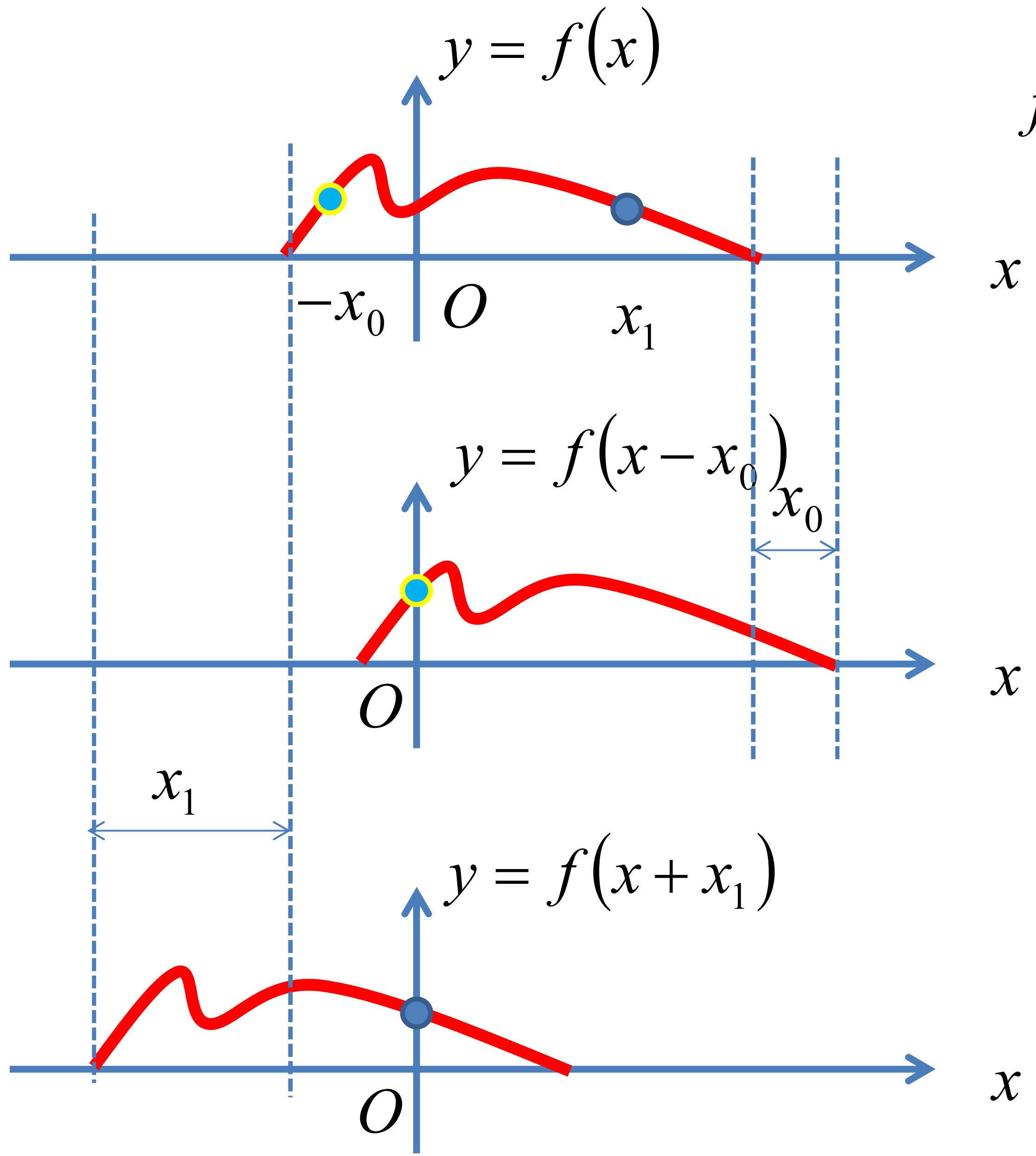
函数平移和反褶

- 函数平移
- 函数反褶





函数移位

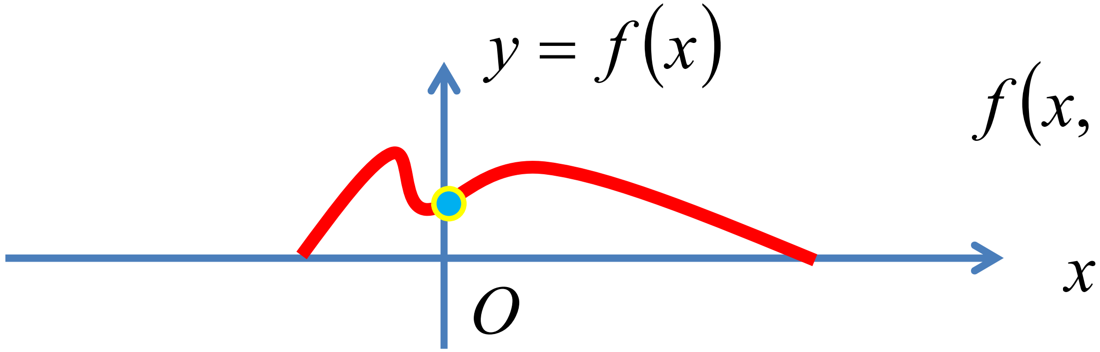


$$f(x, y) = 0$$

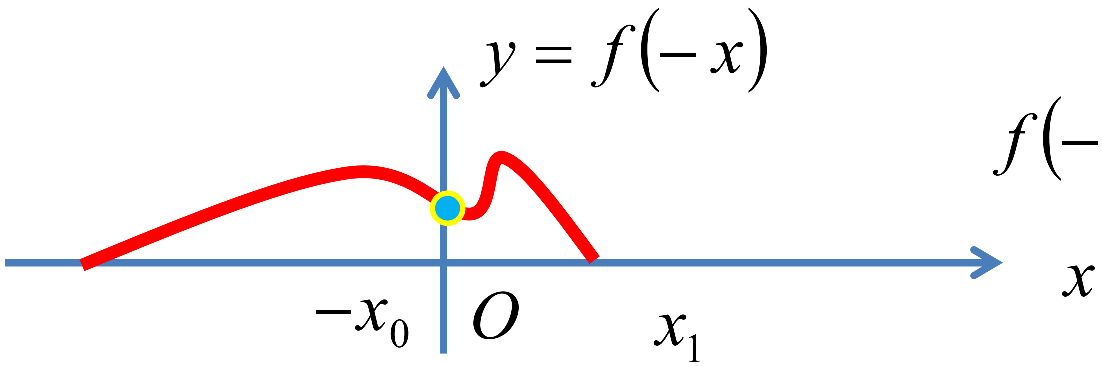
$$f(x - x_0, y) = 0$$

$$f(x + x_1, y) = 0$$

函数反褶



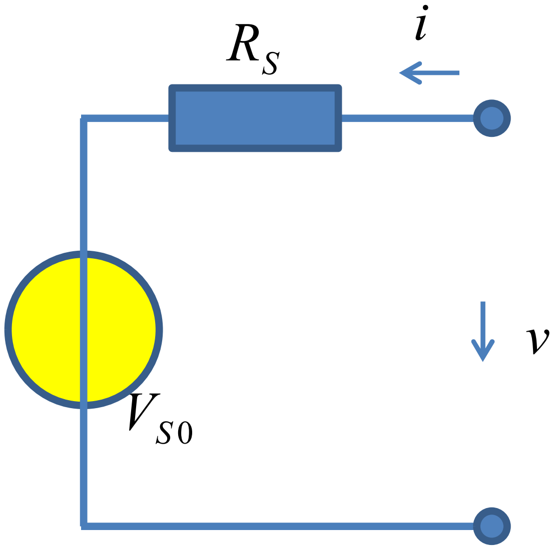
$$f(x, y) = 0$$

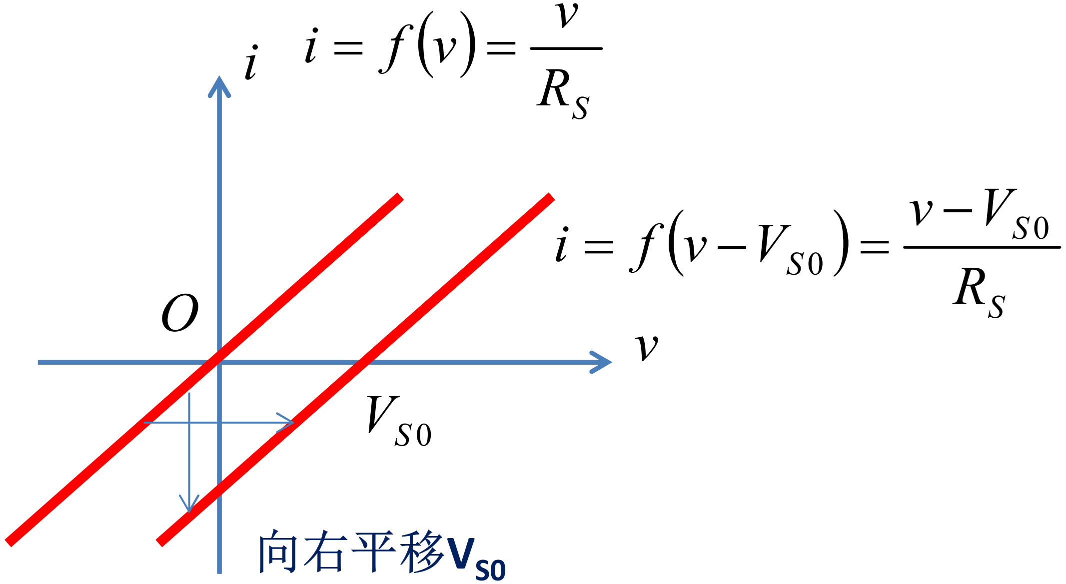


$$f(-x, y) = 0$$

电路例：移位

$$f(x)=\frac{x}{R_S}$$





$$v=V_{S0}+iR_S$$

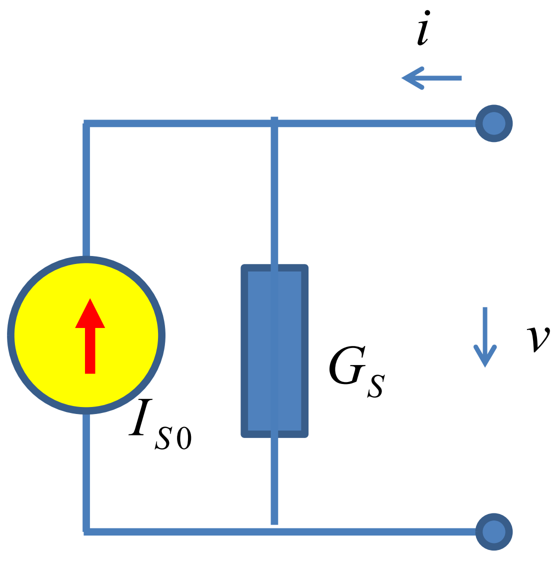
电阻的基础上，加恒压源，向右平移

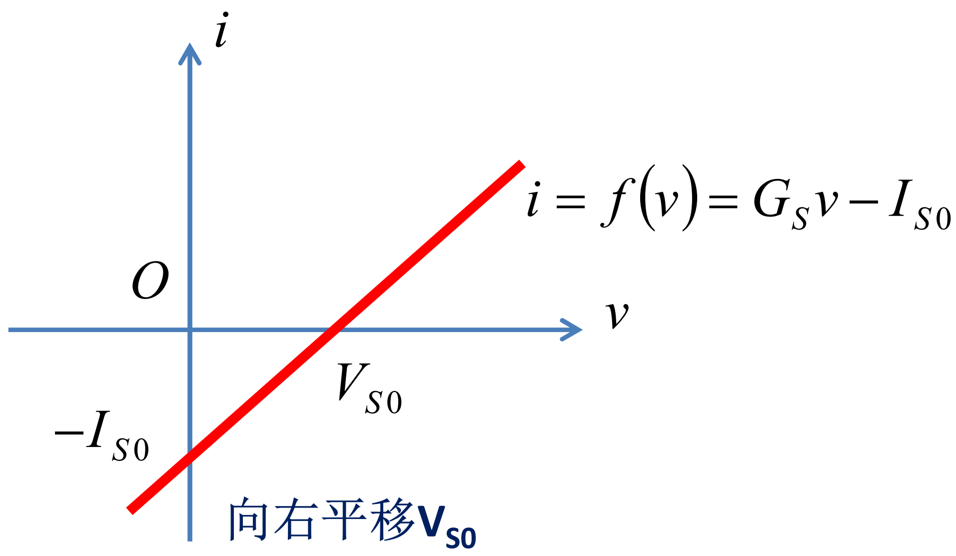
$$\frac{v}{R_S}=\frac{V_{S0}}{R_S}+i=i+I_{S0}$$

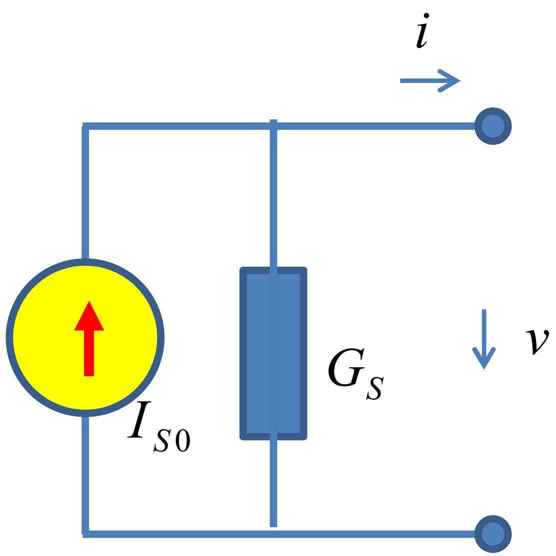
电阻的基础上，加恒流源，向下平移

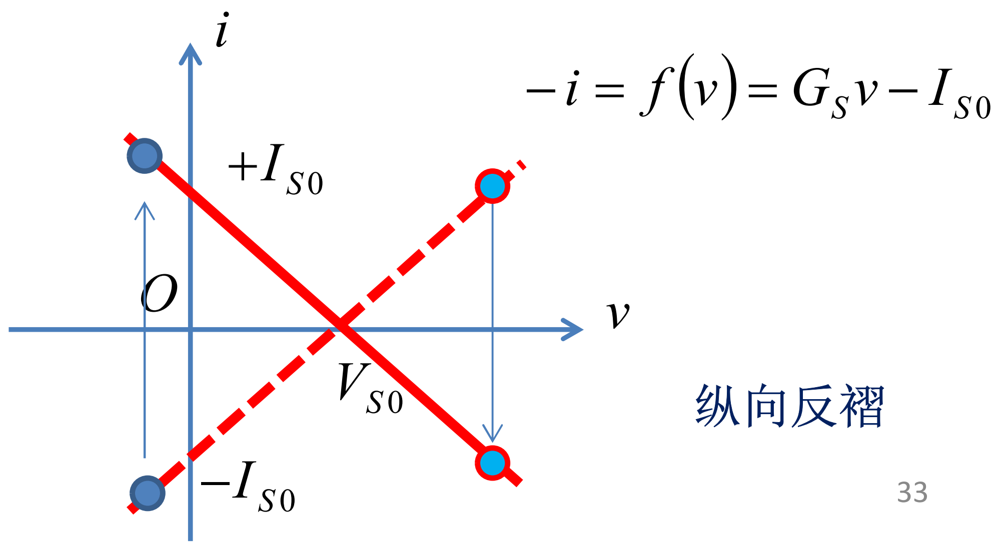
电路例：反褶

$$f(x) = G_S x - I_{S0}$$

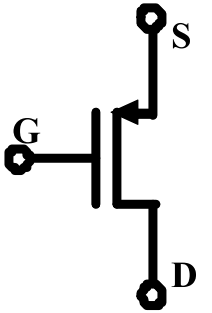


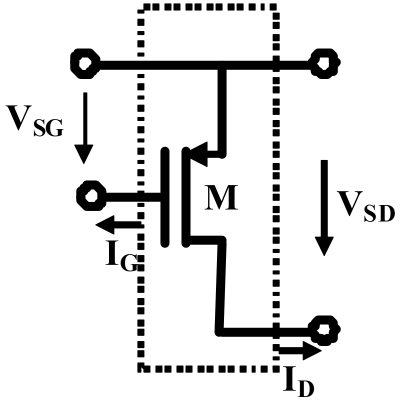


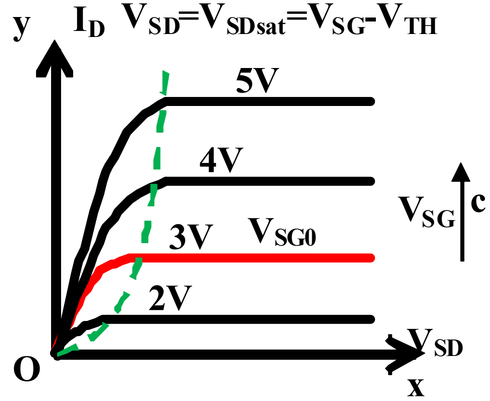




函数平移与反褶运算



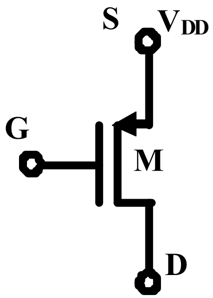


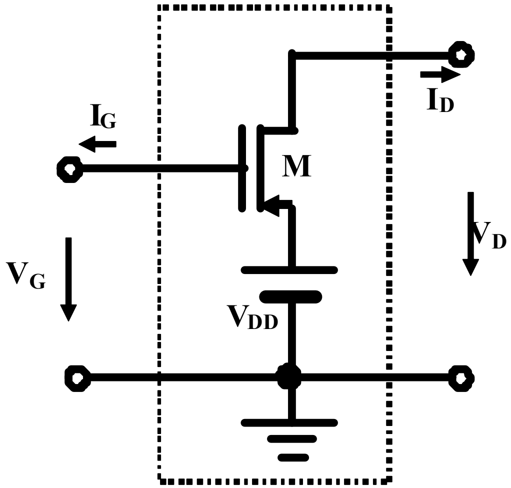


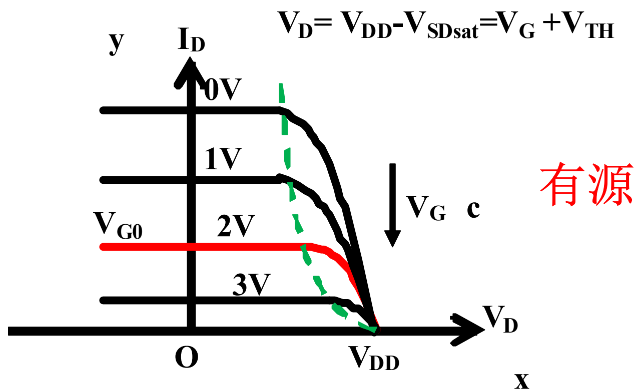
无源

$$V_{DD} = 5V$$
$$V_{TH} = 1V$$

$$I_D = f(V_{SG}, V_{SD}) = f(c, x) = y$$



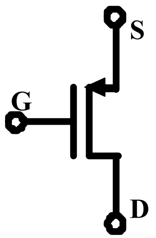


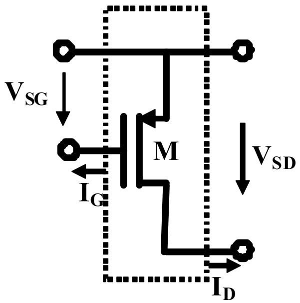


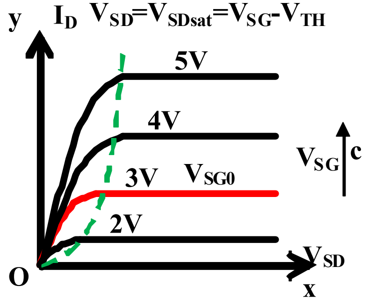
有源

$$I_D = f(V_{DD} - V_G, V_{DD} - V_D) = f(V_{DD} - c, V_{DD} - x) = y$$

先反褶再平移

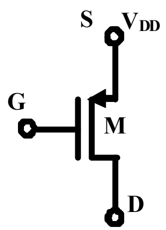


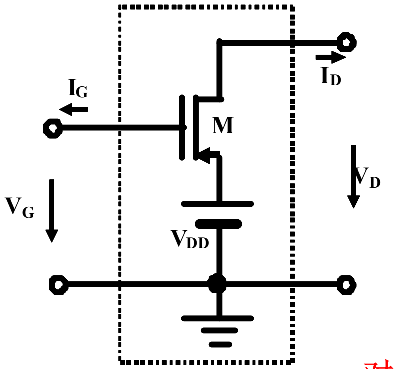


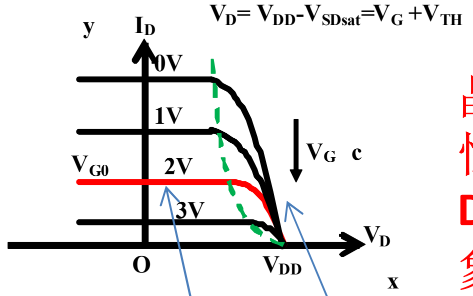


晶体管是非线性电阻
关联参考方向下，**DS**端口伏安特性全部位于一、三象限，只能吸收功率而无法释放功率

$$i_D=\begin{cases}0 & v_{SG}<V_{TH,p}\\ 2\beta_p\left(\left(v_{SG}-V_{TH,p}\right)v_{SD}-0.5v_{SD}^2\right) & v_{SG}>V_{TH,p},v_{DG}>V_{TH,p}\\ \beta_p\left(v_{SG}-V_{TH,p}\right)^2\left(1+\lambda_p v_{SD}\right) & v_{SG}>V_{TH,p},v_{DG}<V_{TH,p}\end{cases}$$







晶体管沟道电阻是电压源的非线性内阻，源关联参考方向下，**DS**端口伏安特性存在位于第一象限的区段，可以在此区段向外释放能量

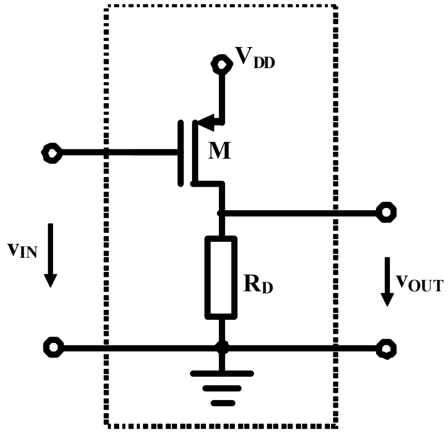
对外等效为恒流源

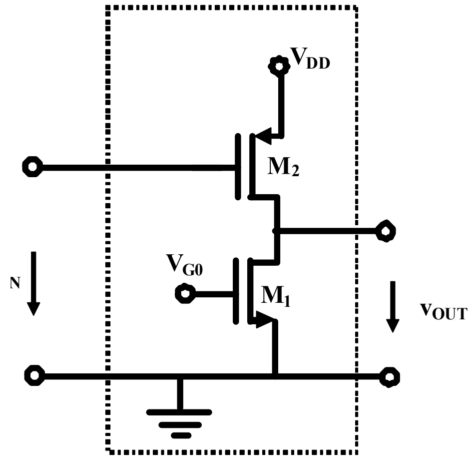
对外等效为有内阻的戴维南源

$$i_D=\begin{cases}0 & v_G>V_{DD}-V_{TH,p}\\ 2\beta_p\left(\left(V_{DD}-v_G-V_{TH,p}\right)\left(V_{DD}-v_D\right)-0.5\left(V_{DD}-v_D\right)^2\right) & v_G<V_{DD}-V_{TH,p},v_D>V_{TH,p}+v_G\\ \beta_p\left(V_{DD}-v_G-V_{TH,p}\right)^2\left(1+\lambda_p\left(V_{DD}-v_D\right)\right) & v_G<V_{DD}-V_{TH,p},v_D<V_{TH,p}+v_G\end{cases}$$

作业3 PMOS反相器

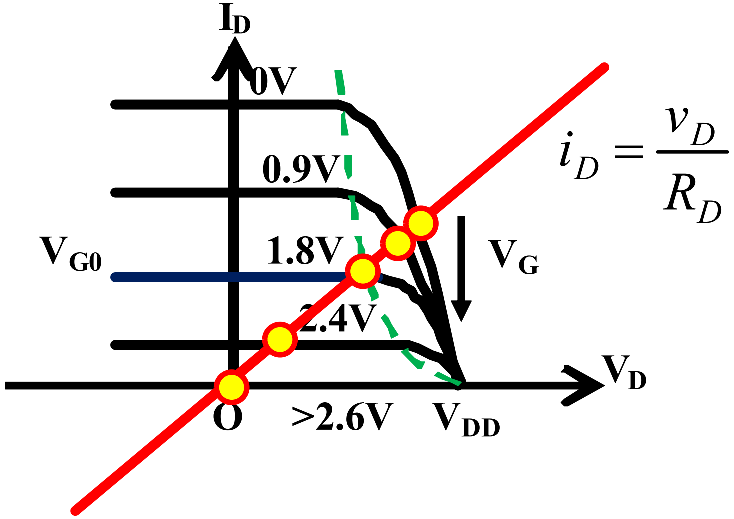
- 请用分段折线法分析如图所示PMOS反相器电路，画出其输入-输出电压转移特性曲线示意图
  - **NMOSFET**参量为**β_n=2.5mA/V^2**，**V_{THn}=0.8V**；**PMOSFET**参量为**β_p=1mA/V^2**，**V_{THp}=0.7V**；偏置电阻**R_D=3.3kΩ**，电源电压**V_{DD}=3.3V**
  - 假设通过某种偏置方式，使得图**b**所示**NMOSFET**的栅极电压被设置为**V_{G0}=1.3V**，源栅电压为**V_{GSn}=1.3V**，过驱动电压为**V_{odn}=V_{GSn}-V_{THn}=0.5V**。

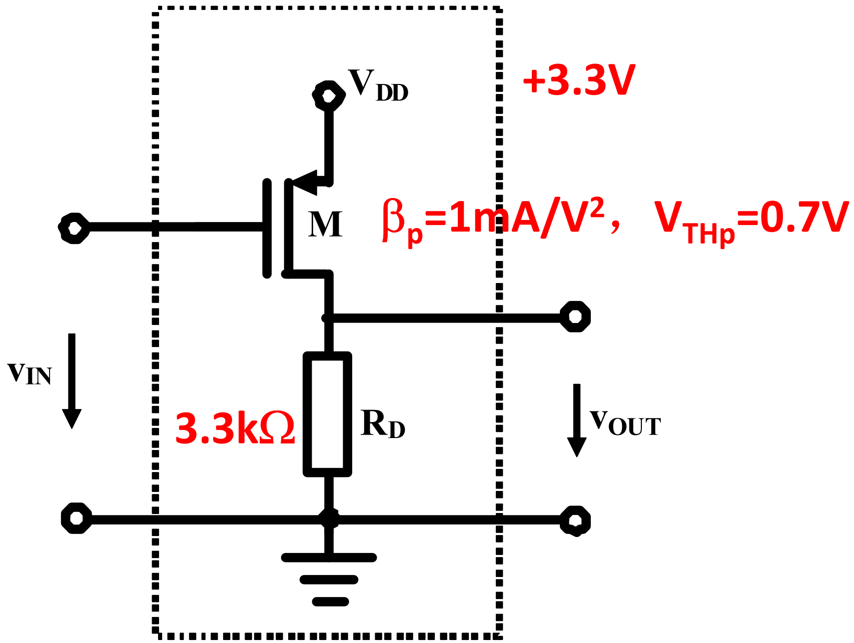




PMOS反相器：图解法原理分析

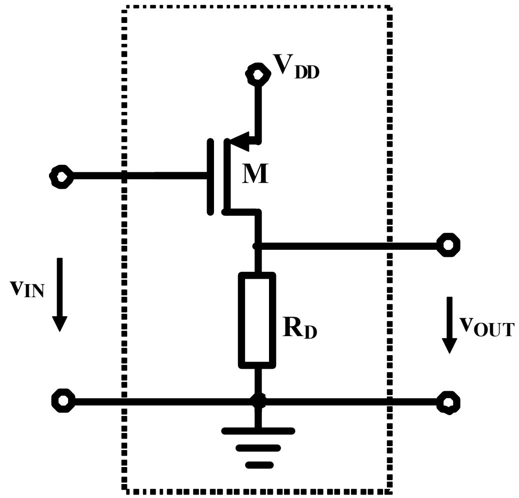
$$i_D = f_{PMOS}\left(V_{DD}-v_G, V_{DD}-v_D\right)$$



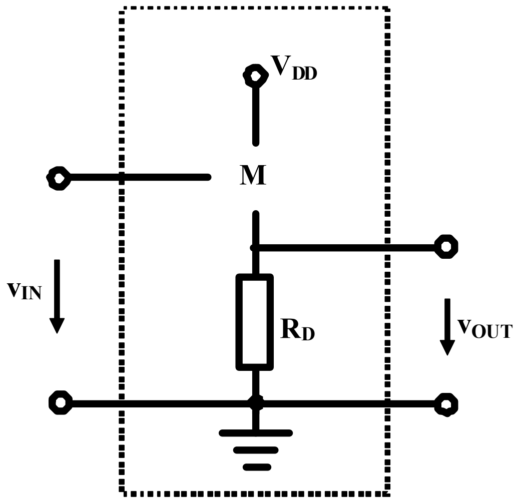


随着输入电压$v_{IN}=v_G$的增加，输出电压$v_{OUT}=v_D$是降低的：反相功能

分段折线：PMOS截止

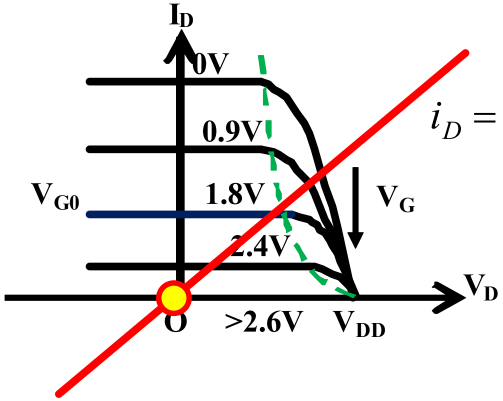


$$v_{IN} > V_{DD} - V_{TH,p} = 3.3 - 0.7 = 2.6V$$



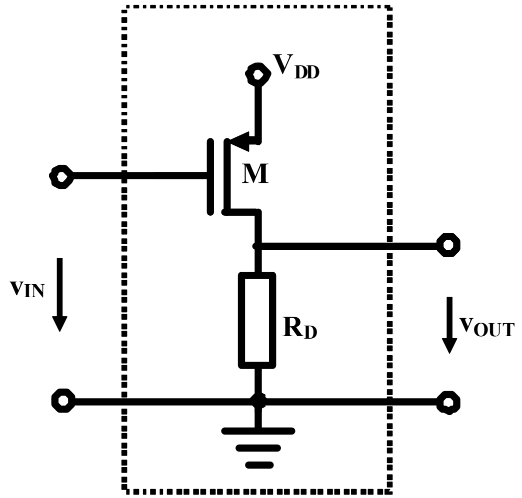
$$v_{OUT} = 0$$

$$i_D = f_{PMOS}\left(V_{DD} - v_G, V_{DD} - v_D\right)$$



$$i_D = \frac{v_D}{R_D}$$

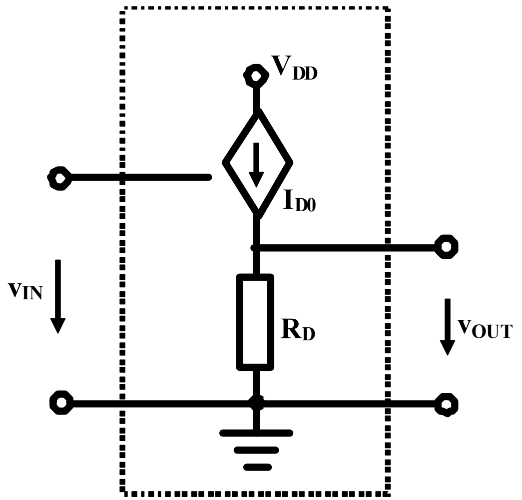
分段折线：PMOS恒流



$$v_{IN} < V_{DD} - V_{TH,p} = 3.3 - 0.7 = 2.6V$$

$$v_{OUT} = v_D < V_{TH,p} + v_G = v_{IN} + 0.7$$

$$I_{D0} = \beta_p \left(V_{DD} - v_{IN} - V_{TH,p}\right)^2 = \left(2.6 - v_{IN}\right)^2 (mA)$$



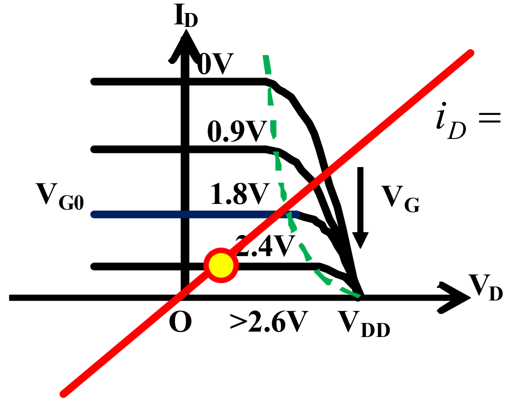
$$v_{OUT} = I_{D0} R_D$$

$$= \beta_p \left(V_{DD} - v_{IN} - V_{TH,p}\right)^2$$

$$= 3.3 \times \left(2.6 - v_{IN}\right)^2$$

输入降低，输出提高

$$i_D = f_{PMOS}\left(V_{DD} - v_G, V_{DD} - v_D\right)$$

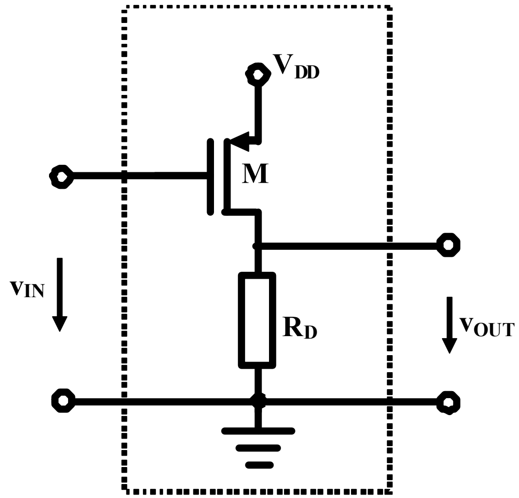


$$i_D = \frac{v_D}{R_D}$$

分段折线

恒流欧姆分界

$$v_{IN} < V_{DD} - V_{TH,p} = 3.3 - 0.7 = 2.6V$$



$$v_{OUT} = v_D < V_{TH,p} + v_G = v_{IN} + 0.7$$

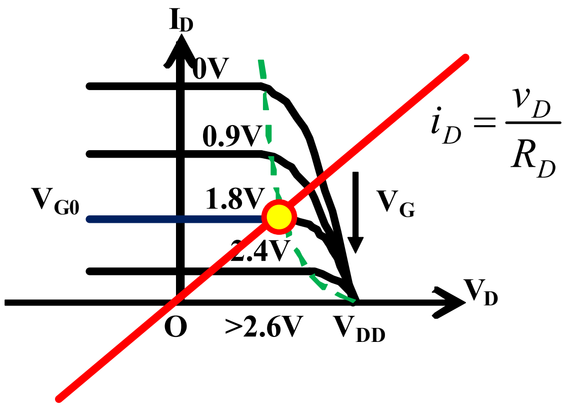
$$v_{OUT} = \beta_p\left(V_{DD} - v_{IN} - V_{TH,p}\right)^2 = 3.3\times\left(2.6 - v_{IN}\right)^2$$

输入降低，输出提高

$$v_{OUT} = \beta_p\left(V_{DD} - v_{IN} - V_{TH,p}\right)^2 = V_{TH,p} + v_{IN}$$

$$= 3.3\times\left(2.6 - v_{IN}\right)^2 = v_{IN} + 0.7$$

$$i_D = f_{PMOS}\left(V_{DD} - v_G, V_{DD} - v_D\right)$$



$$3.3\times\left(2.6 - v_{IN}\right)^2 - v_{IN} - 0.7 = 0$$

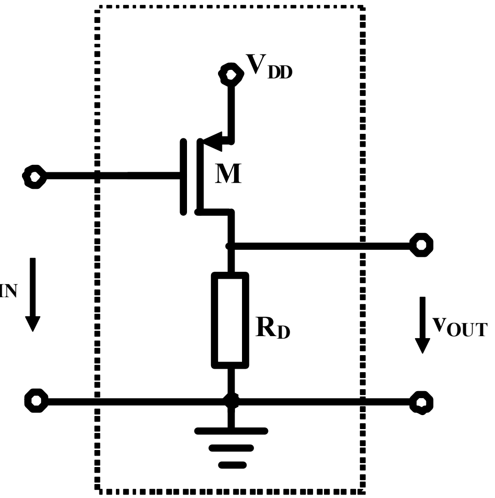
$$3.3v_{IN}^2 - 18.16v_{IN} + 21.608 = 0$$

$$v_{IN} = 1.74V, 3.76V$$

$$v_{IN,k} = 1.74V$$

$$v_{OUT,k} = 2.44V$$

分段折线：PMOS欧姆

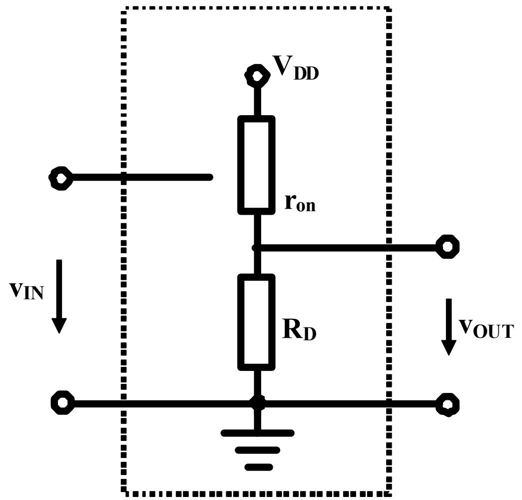


$$v_{IN} < v_{IN,k} = 1.74V$$

$$v_{OUT} = v_D > V_{TH,p} + v_G = v_{IN} + 0.7$$

$$i_D = 2\beta_p\left(\left(V_{DD} - v_G - V_{TH,p}\right)\left(V_{DD} - v_D\right) - 0.5\left(V_{DD} - v_D\right)^2\right)$$

$$\approx 2\beta_p\left(V_{DD} - v_{IN} - V_{TH,p}\right)\left(V_{DD} - v_{OUT}\right) = \frac{V_{DD} - v_{OUT}}{r_{on}}$$



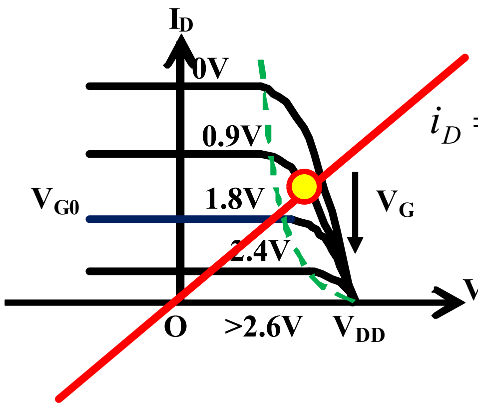
$$v_{OUT} = \frac{R_D}{R_D + r_{on}}V_{DD}$$

$$= \frac{2\beta_p\left(V_{DD} - v_{IN} - V_{TH,p}\right)R_D}{2\beta_p\left(V_{DD} - v_{IN} - V_{TH,p}\right)R_D + 1}V_{DD}$$

$$= \frac{6.6\times\left(2.6 - v_{IN}\right)}{6.6\times\left(2.6 - v_{IN}\right) + 1}V_{DD}$$

$$= \frac{2.6 - v_{IN}}{2.75 - v_{IN}}\times 3.3$$

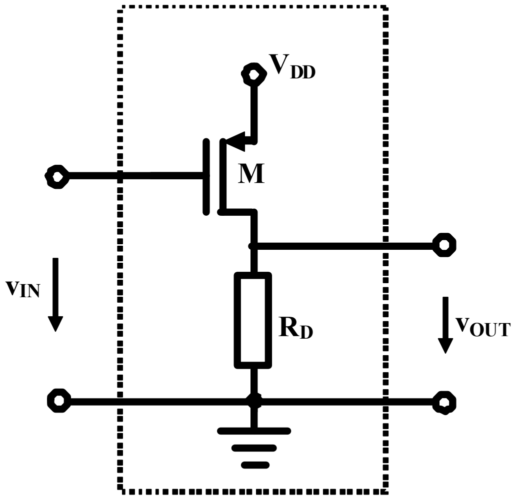
$$i_D = f_{PMOS}\left(V_{DD} - v_G, V_{DD} - v_D\right)$$

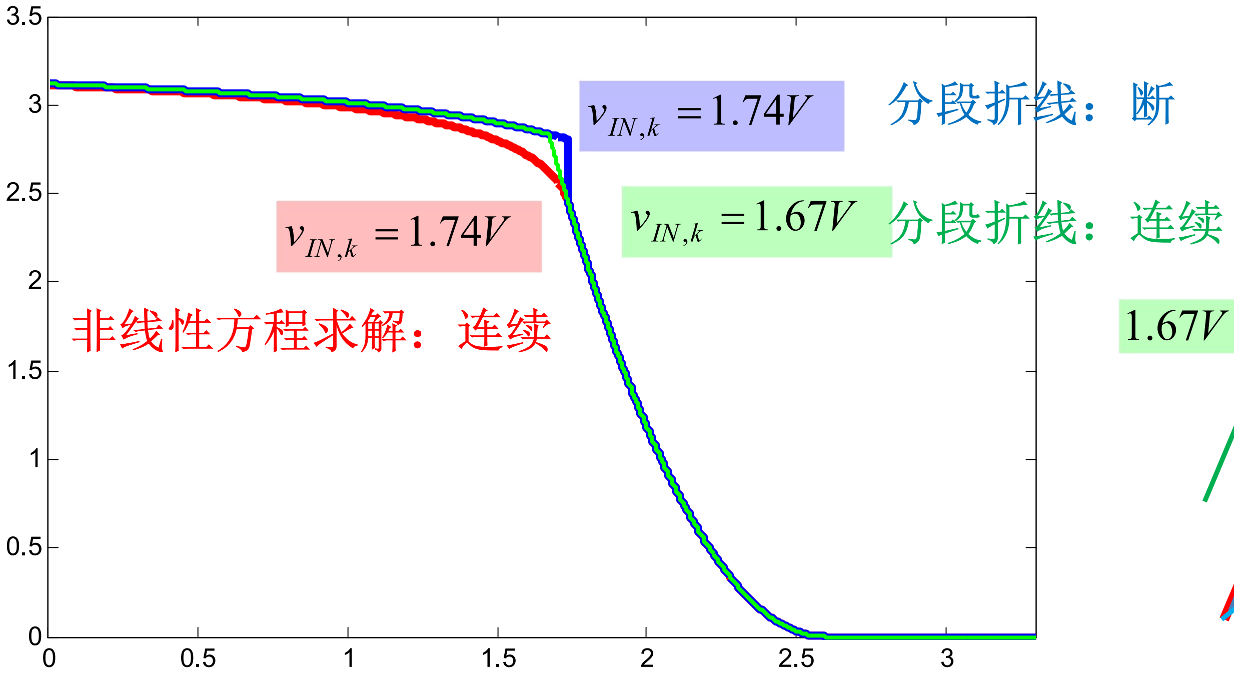


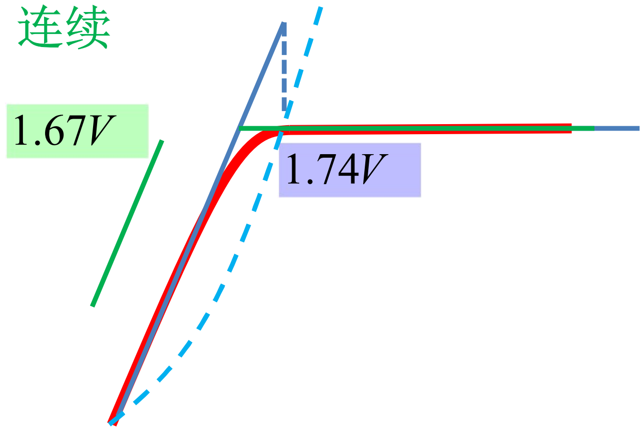
$$i_D = \frac{v_D}{R_D}$$

分段折线分析结果

$$v_{OUT}=\begin{cases}\dfrac{2.6-v_{IN}}{2.75-v_{IN}}\times 3.3 & v_{IN}<1.74V \quad \text{PMOS欧姆导通}\\ 3.3\times(2.6-v_{IN})^2 & 1.74V<v_{IN}<2.6V \quad \text{PMOS恒流导通}\\ 0 & v_{IN}>2.6V \quad \text{PMOS截止}\end{cases}$$

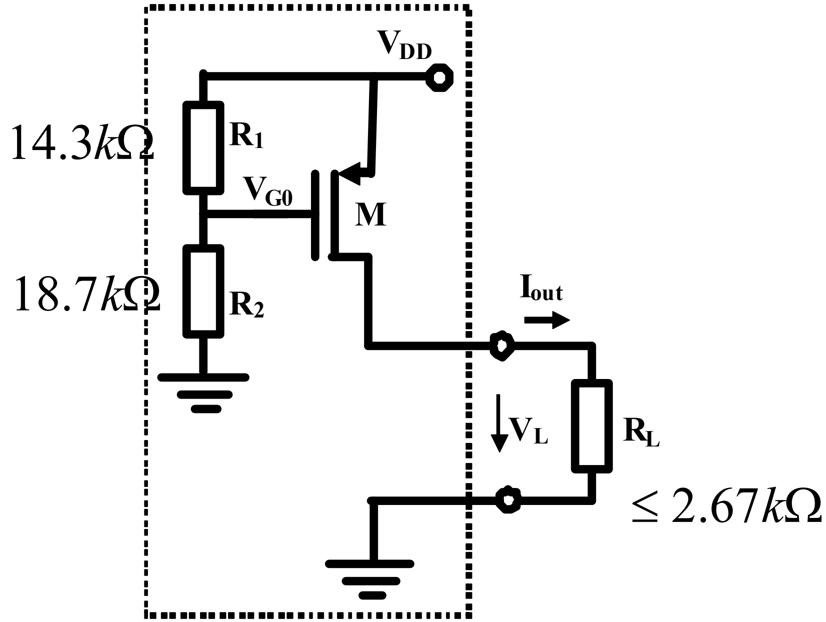




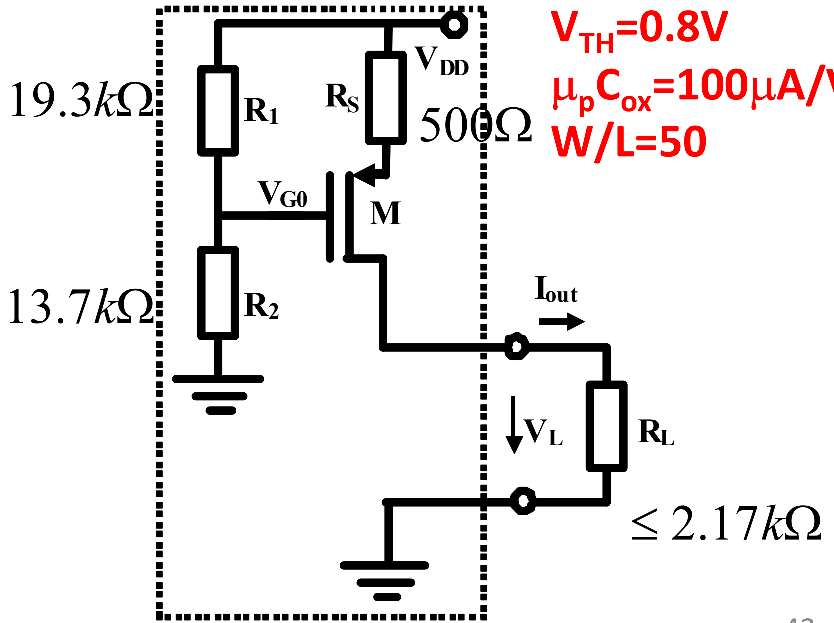


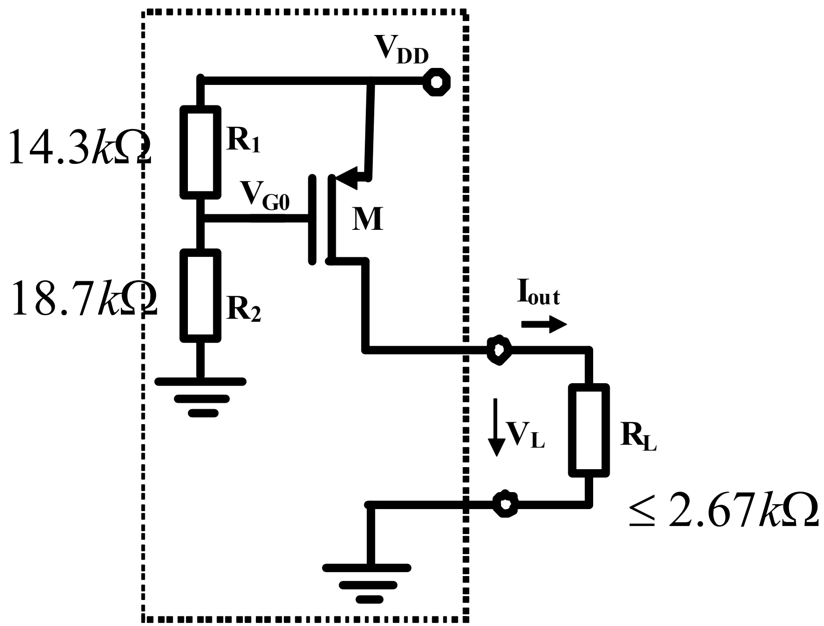
作业4 负反馈降低不确定性

- （1）验证例4设计：确认两个电流源输出电流都是1mA；确认其等效电路为恒流源
- （2）由于工艺参数不确定及环境温度的变化，使得PMOSFET的工艺参量$\mu_p C_{ox}$偏离设计值100μA/V²-5%，请分析确认，图示两个电路结构的等效恒流源输出，有负反馈电阻的输出电流比没有负反馈电阻的输出电流更稳定，更接近设计值1mA



V_{DD}=3.3V
V_{TH}=0.8V
$\mu_p C_{ox}$=100μA/V²
W/L=50



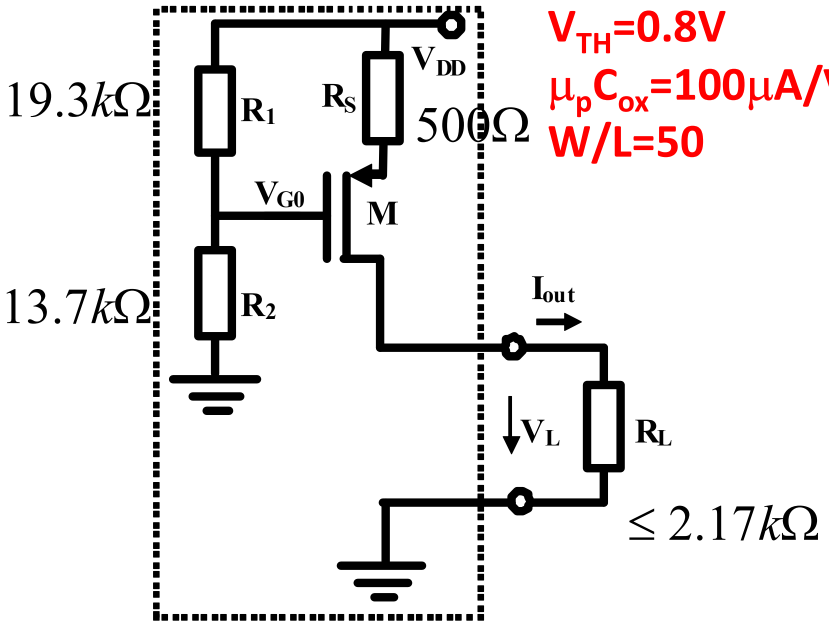


$$V_{G0}=\frac{18.7}{18.7+14.3}\times 3.3=1.87V$$

$$V_{SG}=V_{DD}-V_{G0}=3.3-1.87=1.43V$$

$$I_D=\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG}-V_{TH})^2$$

$$=\frac{1}{2}\times 100\mu\times 50\times(1.43-0.8)^2=0.99mA\approx 1mA$$



V_{DD}=3.3V
V_{TH}=0.8V
$\mu_p C_{ox}$=100μA/V²
W/L=50

$$V_{G0}=\frac{13.7}{13.7+19.3}\times 3.3=1.37V$$

$$V_{SG}=V_{DD}-I_D R_S-V_{G0}=1.93-I_D R_S$$

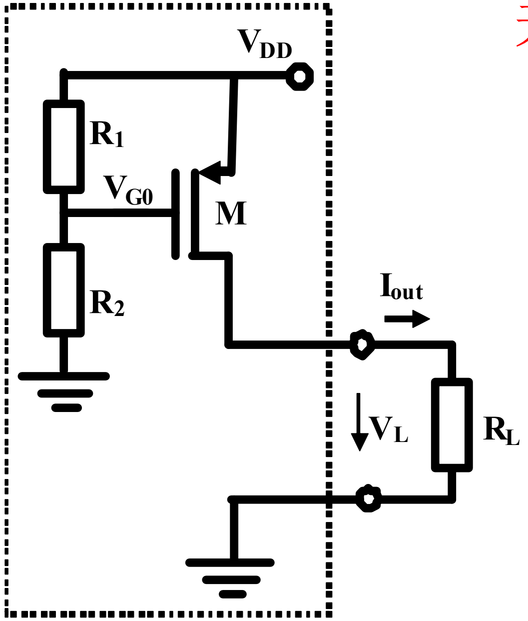
$$I_D=\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG}-V_{TH})^2$$

$$=\frac{1}{2}\times 100\mu\times 50\times(1.93-I_D R_S-0.8)^2=2.5\times(1.13-0.5\cdot I_D)^2$$

$$1.6I_D=(2.26-I_D)^2=5.1076-4.52I_D+I_D^2$$

$$5.1076-6.12I_D+I_D^2=0$$

$$I_D=0.997mA,\quad 5.123mA$$



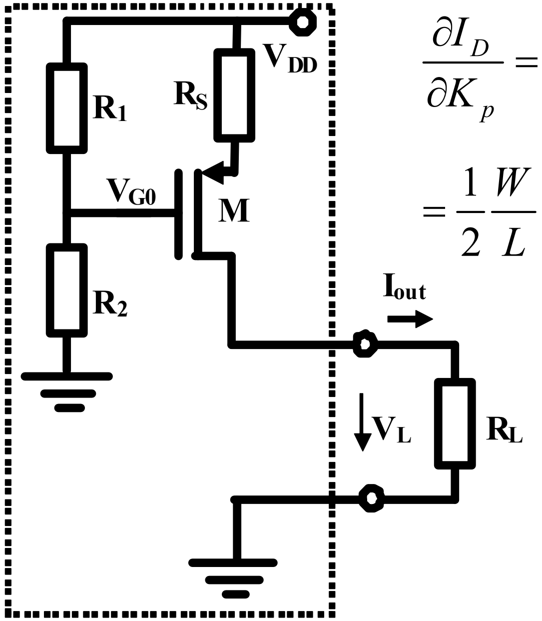
无负反馈

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG}-V_{TH}\right)^2 = \frac{1}{2}K_p\frac{W}{L}\left(V_{SG}-V_{TH}\right)^2$$

$$S_{K_p}^{I_D} = \frac{\partial I_D}{\partial K_p}\frac{K_p}{I_D} = \frac{1}{2}\frac{W}{L}\left(V_{SG}-V_{TH}\right)^2\frac{K_p}{I_D} = 1$$

有串联负反馈电阻

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}\left(V_{SG}-V_{TH}\right)^2 = \frac{1}{2}K_p\frac{W}{L}\left(\eta V_{DD}-I_D R_S-V_{TH}\right)^2$$



$$\frac{\partial I_D}{\partial K_p} = \frac{1}{2}\frac{W}{L}\left(\eta V_{DD}-I_D R_S-V_{TH}\right)^2 + \frac{1}{2}K_p\frac{W}{L}2\left(\eta V_{DD}-I_D R_S-V_{TH}\right)\left(-R_S\frac{\partial I_D}{\partial K_p}\right)$$

$$= \frac{1}{2}\frac{W}{L}\left(\eta V_{DD}-I_D R_S-V_{TH}\right)^2 + g_m\left(-R_S\frac{\partial I_D}{\partial K_p}\right)$$

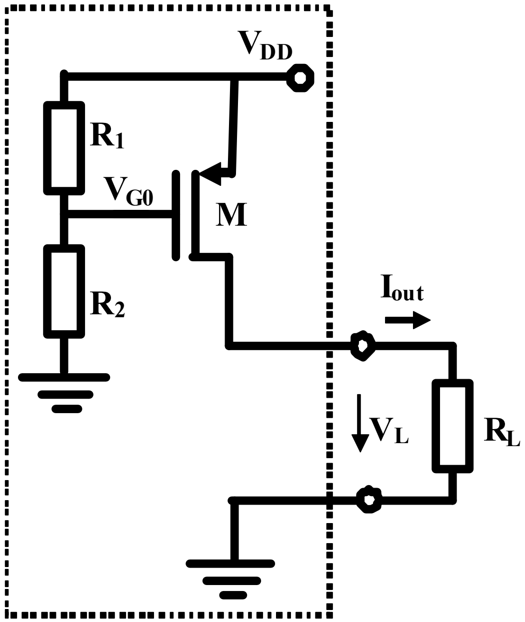
$$g_m = \frac{\partial I_D}{\partial V_{SG}}$$

$$\frac{\partial I_D}{\partial K_p} = \frac{\frac{1}{2}\frac{W}{L}\left(\eta V_{DD}-I_D R_S-V_{TH}\right)^2}{1+g_m R_S}$$

$$S_{K_p}^{I_D} = \frac{\partial I_D}{\partial K_p}\frac{K_p}{I_D} = \frac{1}{1+g_m R_S}$$

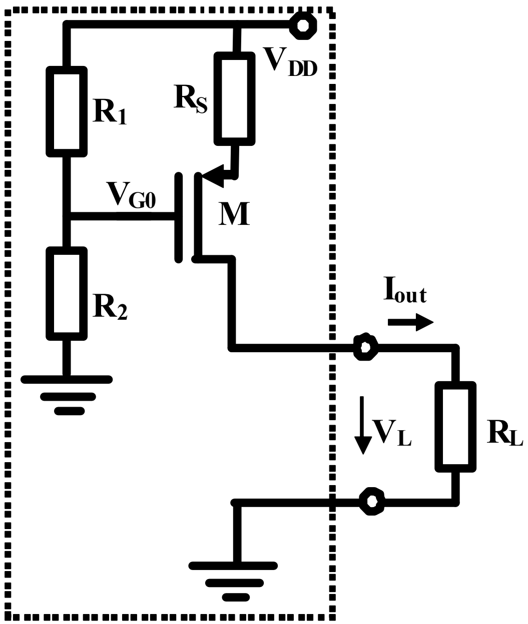
灵敏度因负反馈降低

变化百分比



$$S_{K_p}^{I_D}=\frac{\partial I_D}{\partial K_p}\frac{K_p}{I_D}=1$$

$$\frac{\Delta I_D}{I_D}=S_{K_p}^{I_D}\frac{\Delta K_p}{K_p}=1\times(-5\%)=-5\%$$



$$I_D=\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG}-V_{TH})^2=\frac{1}{2}K_p\frac{W}{L}(V_{SG}-V_{TH})^2$$

$$g_m=\frac{\partial I_D}{\partial V_{SG}}=\mu_p C_{ox}\frac{W}{L}(V_{SG}-V_{TH})=\frac{2I_D}{V_{SG}-V_{TH}}=\frac{2\times 1mA}{1.43-0.8}=3.17mS$$

$$S_{K_p}^{I_D}=\frac{\partial I_D}{\partial K_p}\frac{K_p}{I_D}=\frac{1}{1+g_m R_S}=\frac{1}{1+3.17mS\times 0.5k\Omega}=\frac{1}{1+1.59}=0.39$$

$$\frac{\Delta I_D}{I_D}=S_{K_p}^{I_D}\frac{\Delta K_p}{K_p}=0.39\times(-5\%)=-1.9\%$$

灵敏度代表影响力

$$S_{x_i}^{y} = \frac{\Delta y / y}{\Delta x_i / x_i} \overset{\Delta x_i \to 0}{=} \frac{x_i}{y} \frac{\partial y}{\partial x_i}$$

设计值　实际制作偏离设计值

$$y = f(x_1, x_2, \ldots, x_n) = f(x_{10} + \Delta x_1, x_{20} + \Delta x_2, \ldots, x_{n0} + \Delta x_n)$$

$$= f(x_{10}, x_{20}, \ldots, x_{n0}) + \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \ldots + \frac{\partial f}{\partial x_n}\Delta x_n + h.o.t$$

$$\Delta y = y - y_0 \approx \frac{\partial f}{\partial x_1}\Delta x_1 + \frac{\partial f}{\partial x_2}\Delta x_2 + \ldots + \frac{\partial f}{\partial x_n}\Delta x_n$$

导致输出偏离设计值

$$\frac{\Delta y}{y_0} \approx \frac{\partial f}{\partial x_1}\frac{x_{10}}{y_0}\frac{\Delta x_1}{x_{10}} + \frac{\partial f}{\partial x_2}\frac{x_{20}}{y_0}\frac{\Delta x_2}{x_{20}} + \ldots + \frac{\partial f}{\partial x_n}\frac{x_{n0}}{y_0}\frac{\Delta x_n}{x_{n0}}$$

$$\frac{\Delta y}{y_0} = S_{x_1}^{y}\frac{\Delta x_1}{x_{10}} + S_{x_2}^{y}\frac{\Delta x_2}{x_{20}} + \ldots + S_{x_n}^{y}\frac{\Delta x_n}{x_{n0}}$$

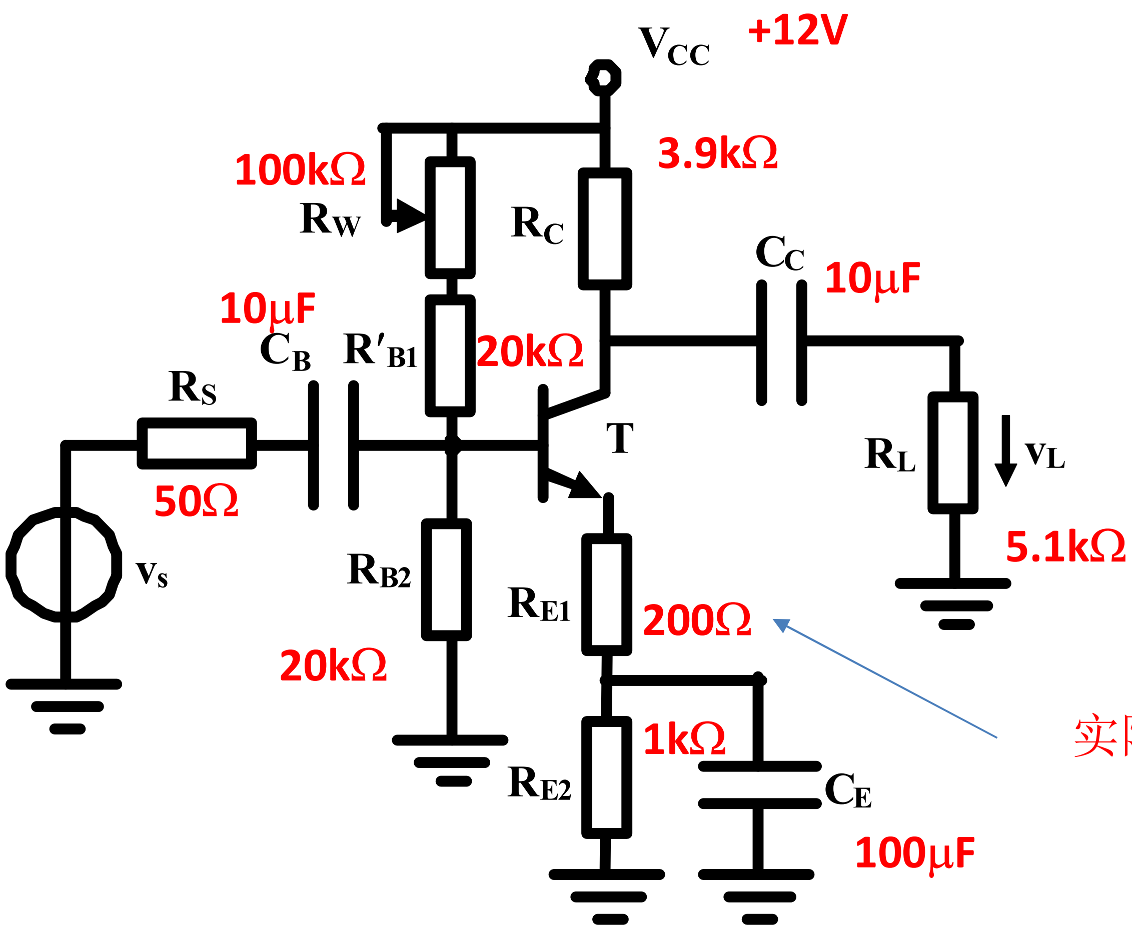
对于极度不稳定因素如β，电路设计时应确保其灵敏度最小，从而提高系统稳定性，负反馈措施可以有效降低灵敏度

灵敏度：该因素对最终输出的影响力大小

单管放大实验电路的说明

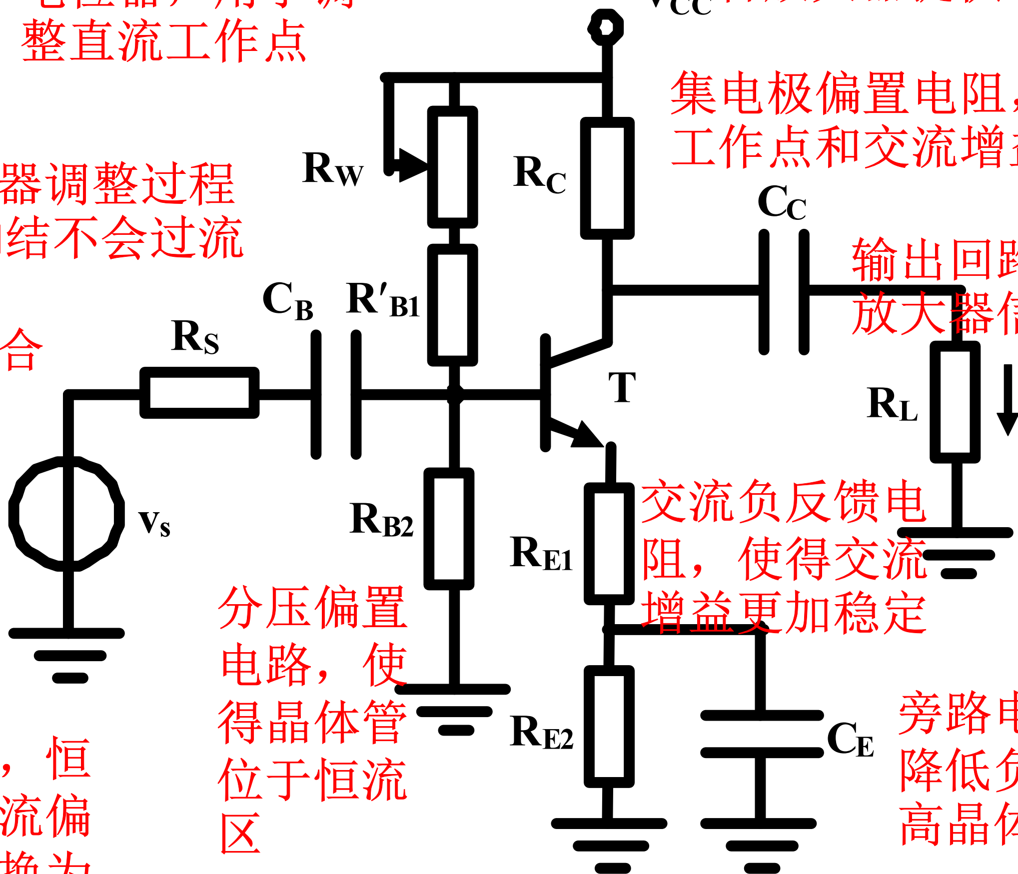
- 实验目的
  - 掌握放大电路直流工作点的调整与测量方法
  - 掌握放大电路主要性能指标的测量方法
  - 了解直流工作点对放大电路动态特性的影响
  - 掌握发射极负反馈电阻对放大电路性能的影响
  - 了解信号源内阻R_s对放大电路频带（上限截止频率f_H）的影响

实验电路



实际电路存在交流负反馈电阻

器件功能描述



直流偏置电压源，为晶体管放大器提供电能供给

电位器，用于调整直流工作点

集电极偏置电阻，决定工作点和交流增益

保护电阻，电位器调整过程中确保晶体管**PN**结不会过流

输出回路耦合电容，耦合放大器信号至负载电阻

输入回路耦合电容，耦合信源信号至放大器电路

负载电阻，吸收放大器输出电能，接收放大器放大处理后的信号

交流负反馈电阻，使得交流增益更加稳定

信号源，提供信号激励

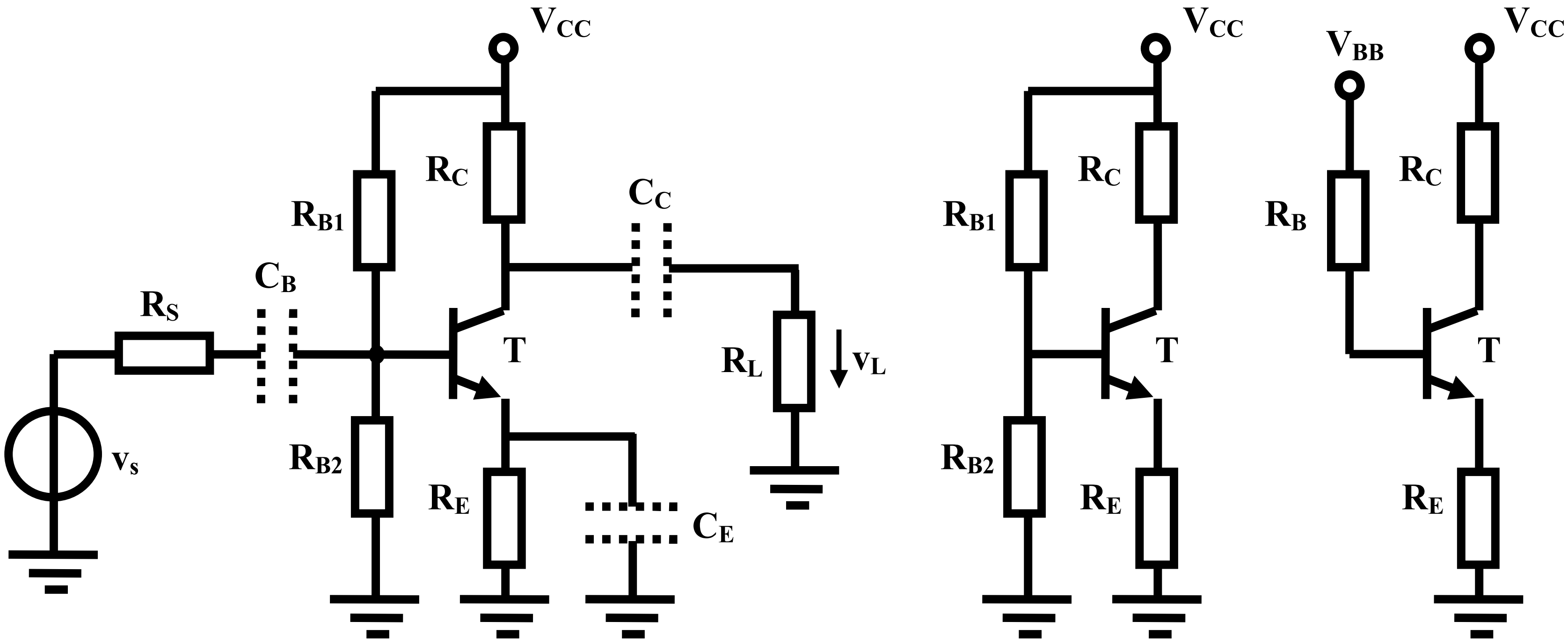
分压偏置电路，使得晶体管位于恒流区

旁路电容，高频短路，降低负反馈作用，提高晶体管高频增益

晶体管：能量转换器件，恒流区晶体管具有吸收直流偏置电压源功率并将其转换为交流信号功率的能力

串联负反馈电阻，用于稳定直流工作点

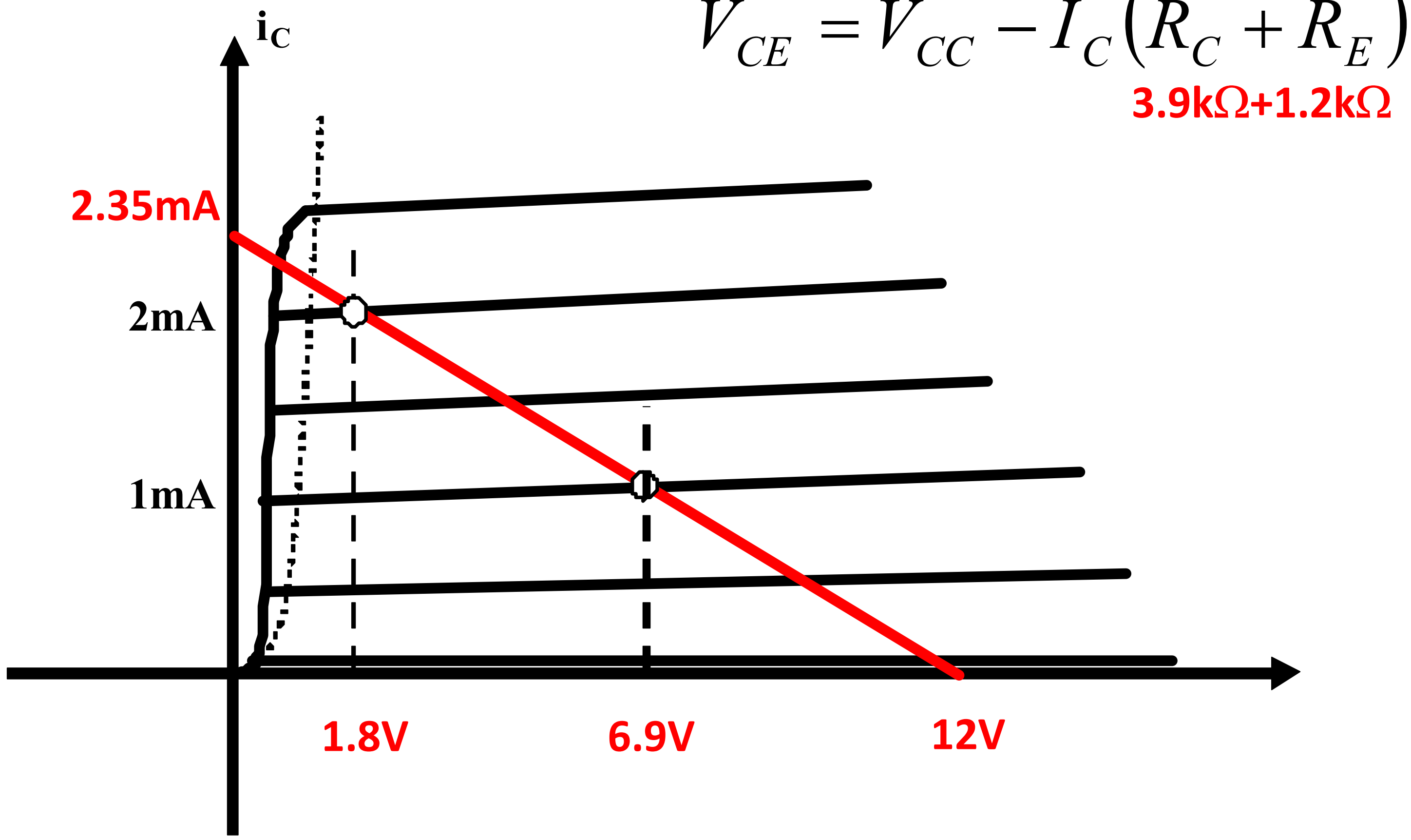
直流工作点的影响
直流负载线



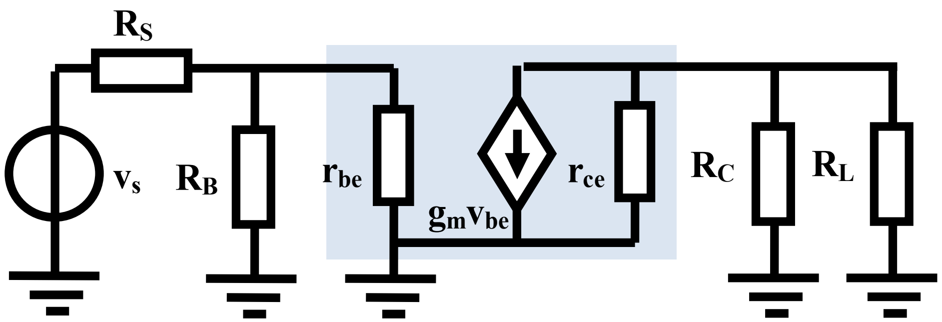
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C\left(R_C + R_E\right)$$

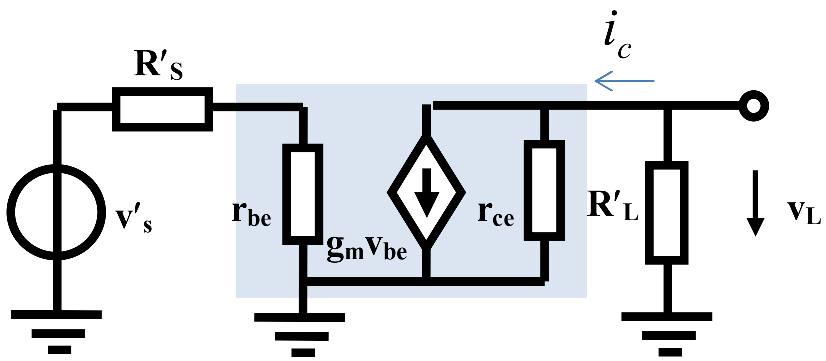
工作点确定

$$V_{CE} = V_{CC} - I_C\left(R_C + R_E\right)$$



交流负载线

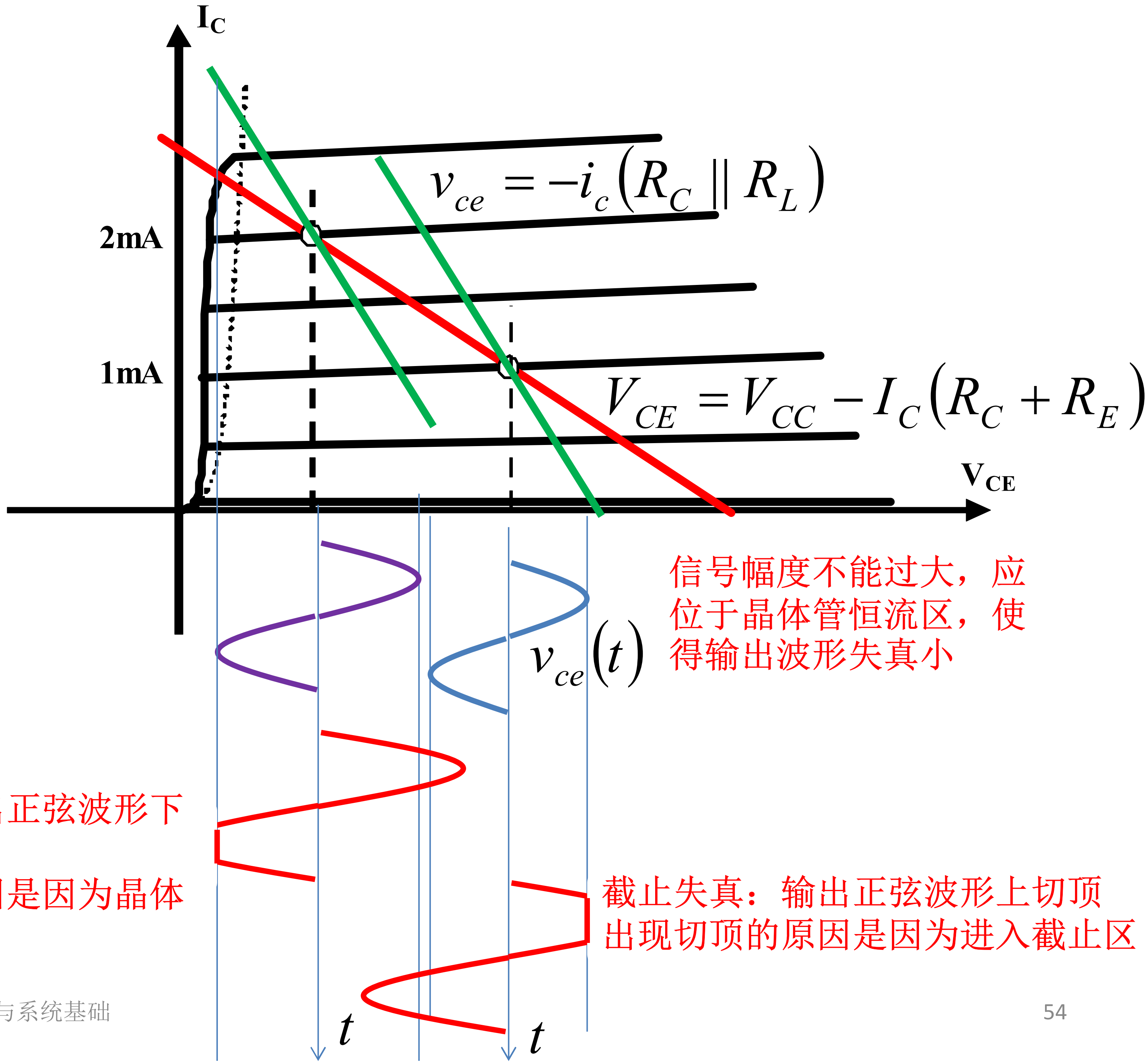




$$v_{ce} = -i_c \left(R_C \parallel R_L \right)$$

3.9kΩ||5.1kΩ=2.2kΩ

交流负载线与大信号失真



信号幅度不能过大，应位于晶体管恒流区，使得输出波形失真小

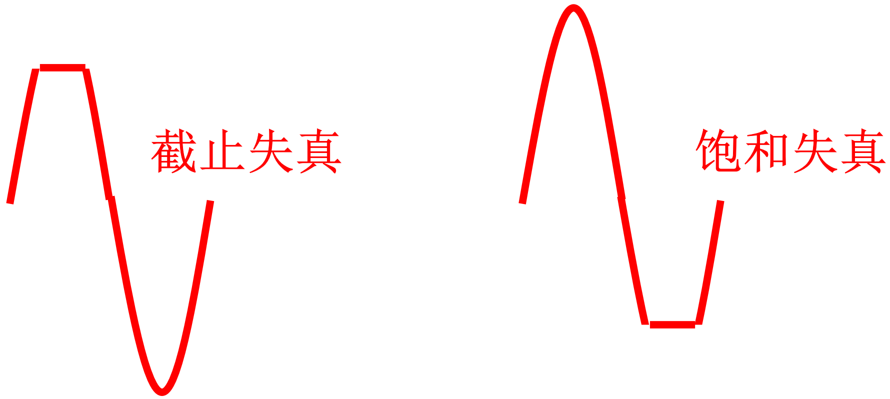
饱和失真：输出正弦波形下切顶

出现切顶的原因是因为晶体管进入饱和区

截止失真：输出正弦波形上切顶

出现切顶的原因是因为进入截止区

失真描述



$$v_{in}(t) = V_{im}\cos\omega_0 t$$

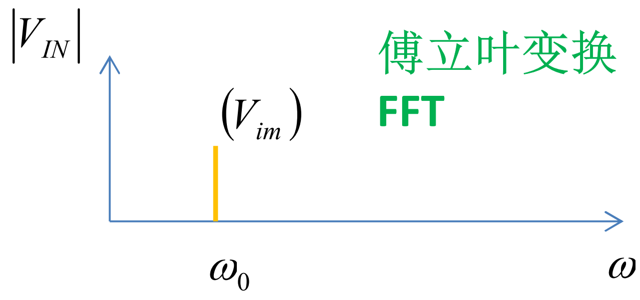
周期激励

基波分量　　　　　　高次谐波分量

$$v_{out}(t) = V_{o0} + V_{om}\cos\omega_0 t + V_{o2}\cos 2\omega_0 t + V_{o3}\cos 3\omega_0 t + \ldots$$

周期响应

正负半周不对称，有直流偏移量

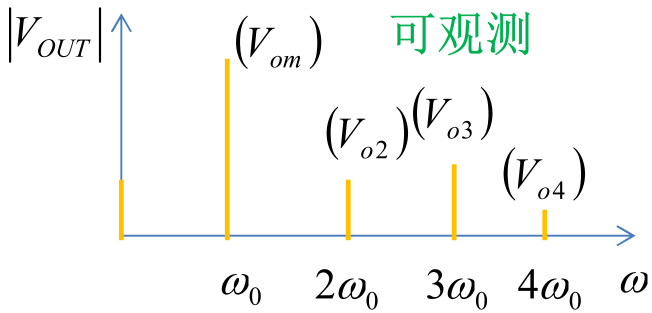


傅立叶变换
FFT

$$THD = 10\log\frac{V_{o2}^2 + V_{o3}^2 + V_{o4}^2 + \ldots}{V_{om}^2}$$

总谐波失真

示波器**FFT**功能可观测



$$HD_2 = 10\log\frac{V_{o2}^2}{V_{om}^2}$$

二次谐波失真

$$HD_3 = 10\log\frac{V_{o3}^2}{V_{om}^2}$$

三次谐波失真

如果示波器**FFT**显示采用**dB**数，基波与高次谐波**dB**数之差就是该次谐波失真大小

线性度描述：可人为给出某种定义

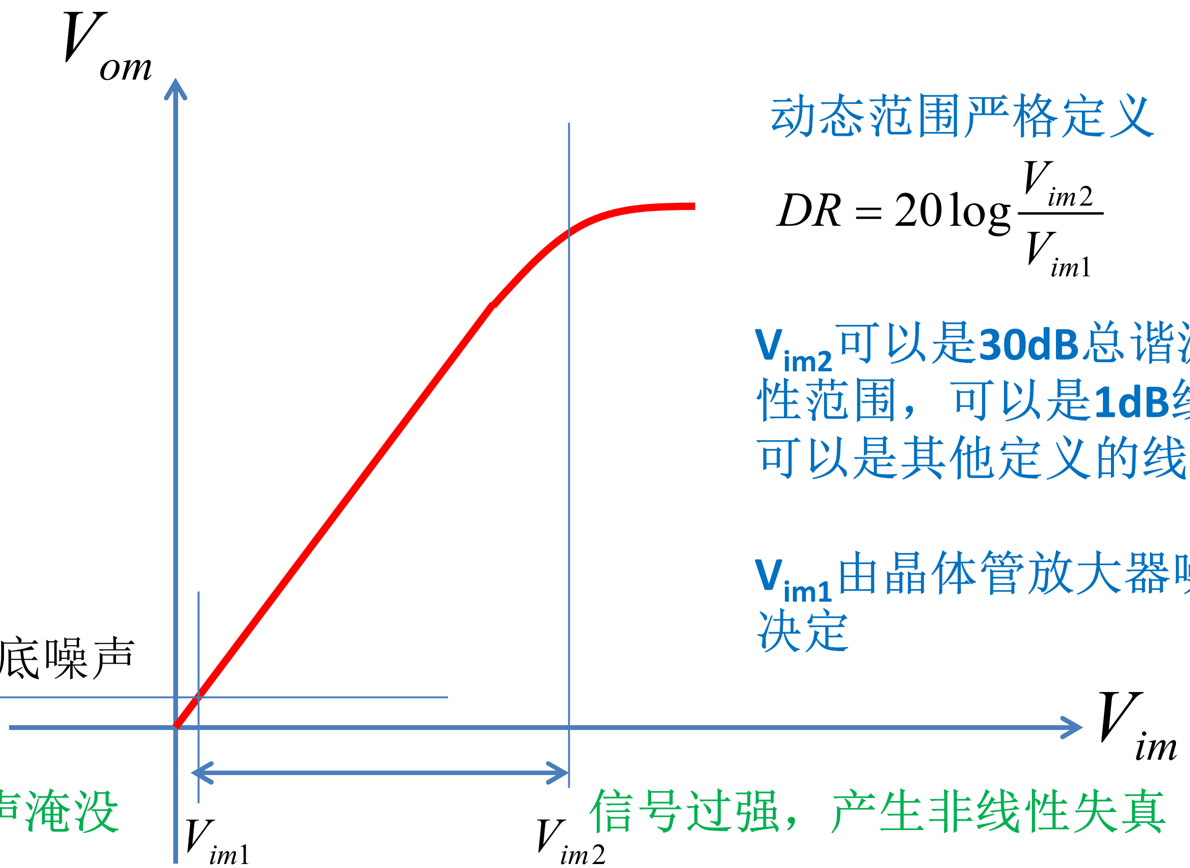
- **1dB**线性范围
  - 在该范围内，微分增益变化不超过**1dB**
    - 有转移特性曲线表达式，易于理论分析
- **30dB**总谐波失真线性范围
  - 正弦波幅度在该范围内变化，总谐波失真小于**30dB** $THD \le -30dB$
    - 方便示波器、频谱分析仪等实际观测

动态范围

$$v_{in}(t) = V_{im}\cos\omega t$$

非线性失真导致

$$v_{out}(t) = V_{om}\cos\omega t + \text{高次谐波分量}$$



信号过小，被噪声淹没

信号过强，产生非线性失真

动态范围严格定义

$$DR = 20\log\frac{V_{im2}}{V_{im1}}$$

V_{im2}可以是**30dB**总谐波失真线性范围，可以是**1dB**线性范围，可以是其他定义的线性范围

V_{im1}由晶体管放大器噪声性能决定

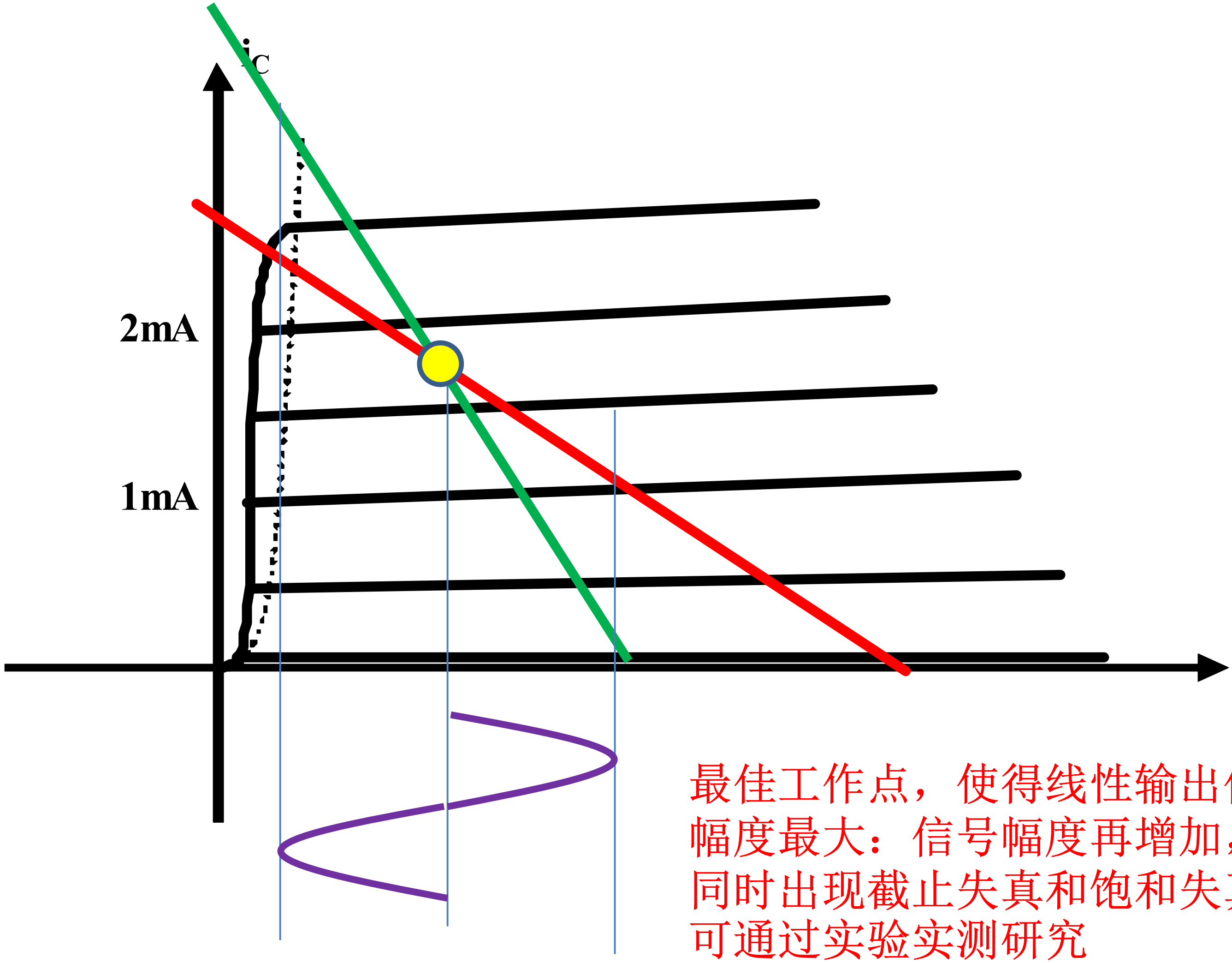
动态范围：信号幅度在该范围内，可认为是接近理想的线性系统

实验教材中的动态范围定义

- 定义高次谐波失真小于**30dB**的信号幅度为线性范围
  - **V_{im1}**不好测量，这里不测
  - **V_{im2}**定义为 $HD_2 < -30dB$ $HD_3 < -30dB$ $HD_4 < -30dB$
  - 称**V_{im2}-V_{im1}≈V_{im2}**为动态范围
    - 方便称呼，非动态范围的严格定义
    - 动态范围严格定义

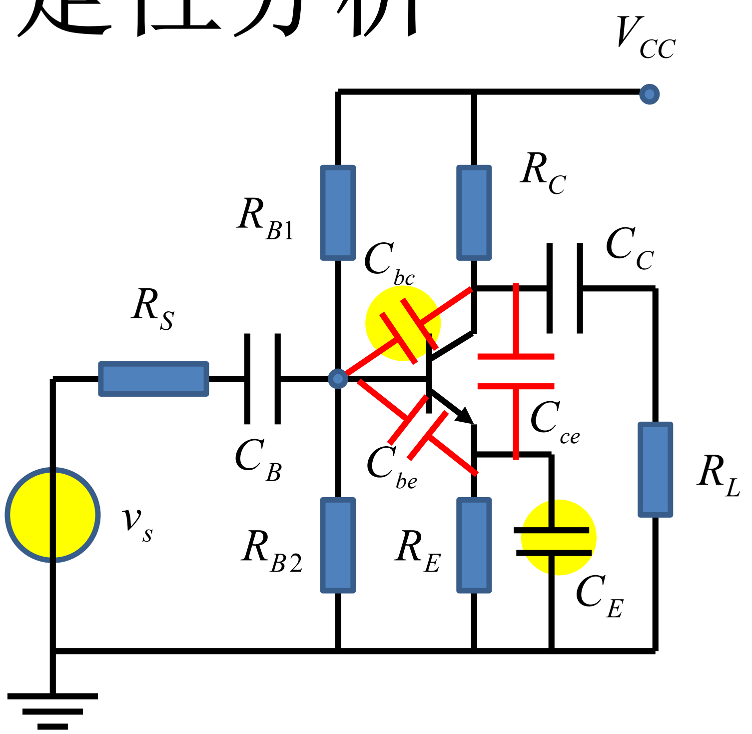
$$DR = 20\log\frac{V_{im2}}{V_{im1}}$$

线性范围最大的最佳工作点



最佳工作点，使得线性输出信号幅度最大：信号幅度再增加，会同时出现截止失真和饱和失真：可通过实验实测研究

带宽形成的定性分析



频率很低时

C_B开路，信号无法通过

C_C开路，信号无法通过

C_E开路，信号增益很小

$$v_s(t)=V_{im}cos(\omega t)$$

$$v_L(t)=V_{om}cos(\omega t+\varphi)$$

$$|A_0|=\frac{V_{om}}{V_{im}}$$

频率极高时

C_{be}短路，输入端信号接地，信号被短接于地

C_{ce}短路，输出端信号接地，信号被端接于地

C_{bc}短路，跨导器作用消失，不具放大作用

位于中间频段时

C_B、C_C、C_E大电容，高频短路

C_{be}、C_{ce}、C_{bc}小电容，低频开路

电路中不考虑电容效应，就是理论课CE组态放大器电路分析结果